PREFACE

In a bid to standardize higher education in the country, the University Grants Commission (UGC) has introduced Choice Based Credit System (CBCS) based on five types of courses viz. *core, discipline specific, generic elective, ability and skill enhancement* for graduate students of all programmes at Honours level. This brings in the semester pattern, which finds efficacy in sync with credit system, credit tranafer, comprehensive continuous assessments and a graded pattern of evaluation. The objective is to offer learners ample flexibility to choose from a wide gamut of courses, as also to provide them lateral mobility between various educational institutions in the country where they can carry their acquired credits. I am happy to note that the University has been recently accredited by National Assessment and Accreditation Council of India (NAAC) with grade "A".

UGC (Open and Distance Learning Programmes and Online Programmes) Regulations, 2020 have mandated compliance with CBCS for U. G. programmes for all the HEIs in this mode. Welcoming this paradigm shift in higher education, Netaji Subhas Open University (NSOU) has resolved to adopt CBCS from the academic session 2021-22 at the Under Graduate Degree Programme level. The present syllabus, framed in the spirit of syllabi recommended by UGC, lays due stress on all aspects envisaged in the curricular framework of the apex body on higher education. It will be imparted to learners over the six semesters of the Programme.

Self Learning Materials (SLMs) are the mainstay of Student Support Services (SSS) of an Open University. From a logistic point of view, NSOU has embarked upon CBCS presently with SLMs in English/Bengali. Eventually, the English version SLMs will be translated into Bengali too, for the benefit of learners. As always, all of our teaching faculties contributed in this process. In addition to this we have also requisitioned the services of best academics in each domain in preparation of the new SLMs. I am sure they will be of commendable academic support. We look forward to proactive feedback from all stakeholders who will participate in the teaching-learning based on these study materials. It has been a very challenging task well executed by the teachers, officers & staff of the University and I heartily congratulate all concerned in the preparation of these SLMs.

I wish you all a grand success.

Professor (Dr.) Ranjan Chakrabarti

Vice-Chancellor

Netaji Subhas Open University

Under Graduate Degree Programme
Choice Based Credit System (CBCS)
Subject : Honours in Physics (HPH)
Course : Laboratory-IV
Course Code : CC-PH-06

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NETAJI SUBHAS OPEN UNIVERSITY

UG : Physics
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Unit 1 ❑ To find the number of lines per centimeter of a transmission grating and to measure the wavelength of an unknow spectral line

Structure

1.0 Objective

To find the number of lines per centimetre of a transmission grating and to measure the wave length of an unknown spectral line.

1.1 Introduction

A grating is a diffractive optical element which contains a large number of equidistant slits of same width. Gratings are fabricated by several techniques: (i) mechanically by ruling equidistant parallel lines on a glass plate by a diamond point, (ii) replica grating produced by depositing a thin film of cellulose acetate on mechanically ruled grating, (iii) optically by interfering two coherent parallel beams on a photosensitive plate. In case of mechanically ruled grating the region where a line is drawn act as an opaque and spaces in between the lines acts as slits. Number of lines on a transmission grating typically is of the order of 15000 per inch.

1.2 Apparatus required

Spectrometer, sodium vapour lamp, grating, spirit level, magnifying glass.

1.3 Theory and formula used

When a parallel beam of monochromatic light produced by the collimator, incident normally on a grating, the beam of light will be diffracted through the grating. On both the sides of central maximum, principal maxima of different orders will be formed.

$$(a + b) \sin \theta = n\lambda \quad \text{..... (1)}$$

where θ is the angle of diffraction corresponding to the nth order principal maximum

The width of transparent portion of the slit is a and width of opaque portion is b, the distance $a + b$ is grating element.

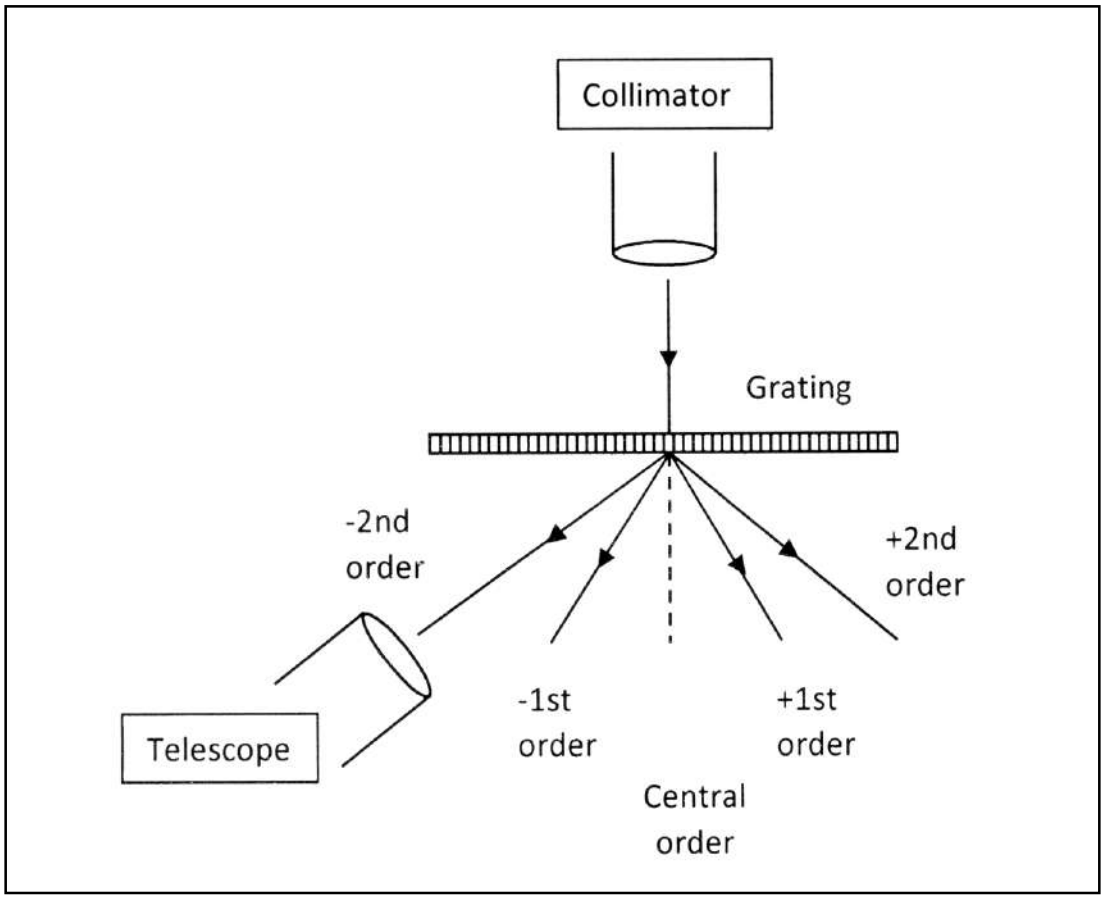


Fig. 1. Diffraction angle measurement.

Grating element is related to is number of rulings per cm of the grating (N) by the relation

$$(a + b) = \frac{1}{N}$$

equation (1) becomes

$$\sin \theta = n\lambda \qquad \text{or} \quad N = \frac{\sin\theta}{n\lambda} \qquad \text{..... (2)}$$

and $$\lambda = \frac{\sin\theta}{Nn} \qquad \text{..... (3)}$$

By measuring θ experimentally, we can find out number of rulings per cm of the grating using equation (2), and wavelength of any unknown spectral line using equation (3).

1.4 Experimental procedure

1. Adjust the telescope and collimator for parallel rays.
2. Level the spectrometer including grating table by a spirit level.
3. Make telescope and collimator in line with each other. Now rotate the telescope through 90°, so that collimator is perpendicular to the axis of the telescope. Keeping grating on the table, rotate the table until telescope receives the image of the slit, and image coincides with intersection of the cross wires. For making grating surface normal to the incident light, rotate the table containing the grating from this position through 45°.
4. Rotate the telescope towards left side of the direct beam to receive the first order spectrum (shown in Fig. 1). Take the reading of the scale of both the verniers. Now rotate the telescope towards right side of the direct beam to observe the first order spectrum on other side of direct beam. Take the readings both the verniers.
5. Similarly set the position of the telescope for observing second order diffracted image on either side of direct beam. Take the reading of both the verniers.
6. Repeat the above procedure.

TABLE 1. Number of lines per cm on the grating

Serial number	Order number (n)	Telescope position												Difference in reading for the same vernier LHS ~ RHS 2θ	Mean 2θ	θ
		LHS of direct beam						RHS of direct beam								
		V_I			V_{II}			V_I			V_{II}					
		MSR	VSR	Total	MSR	VSR	Total	MSR	VSR	Total	MSR	VSR	Total			
1. 2. 3. 4. 5.	1st order															
1. 2. 3. 4. 5.	2nd order															

Calculation

From equation (2), $N = \frac{\sin\theta}{n\lambda}$

For n = 1, $N = \frac{\sin\theta}{\lambda}$ = ...lines/cm

For n = 2, $N = \frac{\sin\theta}{2\lambda}$ = ...lines/cm

Mean N = ... lines/cm

TABLE 2. Wave length of an unknown spectral line

Serial number	Order of number (n)	Telescope position												Difference in reading for the same vernier LHS ~ RHS 2θ	Mean 2θ	θ
		LHS of direct beam						RHS of direct beam								
		V_I			V_{II}			V_I			V_{II}					
		MSR	VSR	Total	MSR	VSR	Total	MSR	VSR	Total	MSR	VSR	Total			
1. 2. 3. 4. 5.	1st order															
1. 2. 3. 4. 5.	2nd order															

Calculation

The value of N is known from previous calculation.

For n = 1, $\lambda = \frac{Sin\theta}{N}$ = ……..nm

For n = 2, $\lambda = \frac{Sin\theta}{2N}$ = ……..nm

Mean wavelength λ = ……..nm

1.5 Observation

Find the vernier constant of the spectrometer

Vernier constant = 1 M.S.D. – 1 V.S.D.

1.6 Result

Number oflines per centimetre of a transmission grating (N) = lines/cm

Wave length CA.) of an unknown spectral line = ... nm

1.7 Precautions

1. The grating surface must be normal to the incident rays.
2. The ruled surface should face the telescope.
3. Do not touch the surface of the grating.

1.8 Oral Questions

1. What is the difference between interference and diffraction?
2. Give an example of diffractive optical element.
3. How grating can be fabricated?
4. How do you set grating for normal incidence?
5. What is grating element?

Unit 2 ❑ To study photo current versus intensity and wanelength of light; maximum photo electrons versus frequency of light

Structure

2.1 Objective

To show light behaves like a particle when a partiele it interacts with matter, such as electrons on a metal serface. And also estimate to the value of Planck's constant *h*.

2.2 Introduction

Photo electgric effect, phenomenon in which electrically charged particles are released from or within a materid when it absorbs electromagnetic radiation. The effect is often defined as the ejection of electrons from a metal plate when light falls on it. The phenomenon was fundamentally significant in the development of modern phy6sics because of the puzzling questions it raised about the nature of light-particle vs wave like behaviour and finally resulved by Albert Einstein in 1905. The effect remains important for research in areas from material science to astrophysics, as well as forming the basis for a variety of useful devices.

2.3 Theory

We known that some every is required to remove the least tightly bound electorus from the mental surface. This minimum energy required to release one electron from the surface is called work function ω_0. The work function is measure of efficiency of the mental to serve as electron emitter. Metals with low ω_0 value are good electron emitters.

e.g Cs, Na, etc.

When an electron at the mental surface absords the energy hv of the incident rediation a certain part is used by the electron to do work equal to ω_0. So as to overcome the attractive forces of the positive ions of the mental. The remaining energy $(hv - \omega_0)$ is—

$$\frac{1}{2}mv_{\max}^2 = hv - \omega_0 \quad \text{..... (1)}$$

where m is mass of the electron & $V_{\max}$ is the maximum speed of mitted electron. This is known as Einstein's Photoelectric equation. The threshold frequencies v_0 for a mental surface is the frequency of photon which is just sufficient to selease an electron from the surface with zero K.E.

so, $0 = hv_0 - \omega_0$

or, $hv_0 = \omega_0$

With this equation (1) takes the form

$$\frac{1}{2}mv\ \max^2 = h(v - v_0)$$

At stopping potential (v_s), there will be h_0 electron at the anode surface. The nagative potential repels all electrons to search the anode surface. All electrons will stop their motion

i.e. $\frac{1}{2}mv\ \max^2 = eV_s$

Therefore, Equation (B) becomes

$$eV_s = h(v - v_0)$$

$$\text{or, } V_s = \frac{h}{e}(\nu - \nu_0) \qquad \ldots\ldots\ldots\ldots (4)$$

So, if we arrange an experiment with varying frequency of incident photon, we get different stopping potential (V_s). Now, if we plot the equation (4) we get a straight line graph as shown in Fig. 2.1.

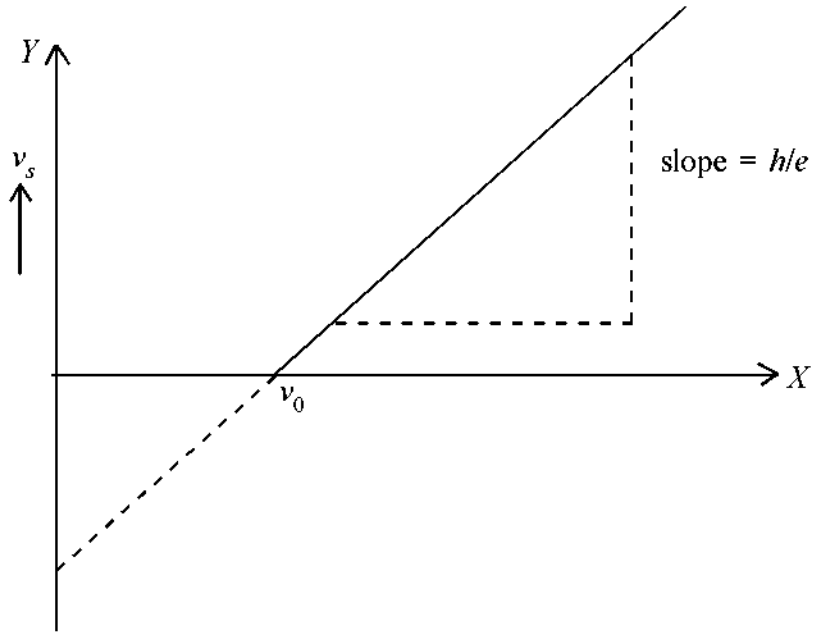


Fig. 2.1

So, slope of this straight line givens the value of $\frac{h}{e}$ from which h is determind. From the interception on the X-axis we get ν_0 and have work function $\omega_0 = h\nu_0$.

Graph of stopping potential (v_s) as a function of incident frequency (ν).

The main light source is an incandescent lamp. The different wavelengths can be selecteted by Nerious filters. Usually the filters of different wevelengths available for this experiment are Red at 690.7 nm, Yellow 579.0 nm, Green at 546.1 nm, Blue at 435.8 nm and violet at 404.7 nm. The filters can be clipped or taped. The inexpensive, looking filters are available commercially for 405 nm, 546 nm and 691 nm.

Again photo electric current increases linearly with increase of intensity of incident light at a fixed frequency and fixed accelerating potential. This aspect can also be verified by blowly varying the intersity in steps and noting the corresponding photoelectric current at a constant frequency and fixed accelerating potential.

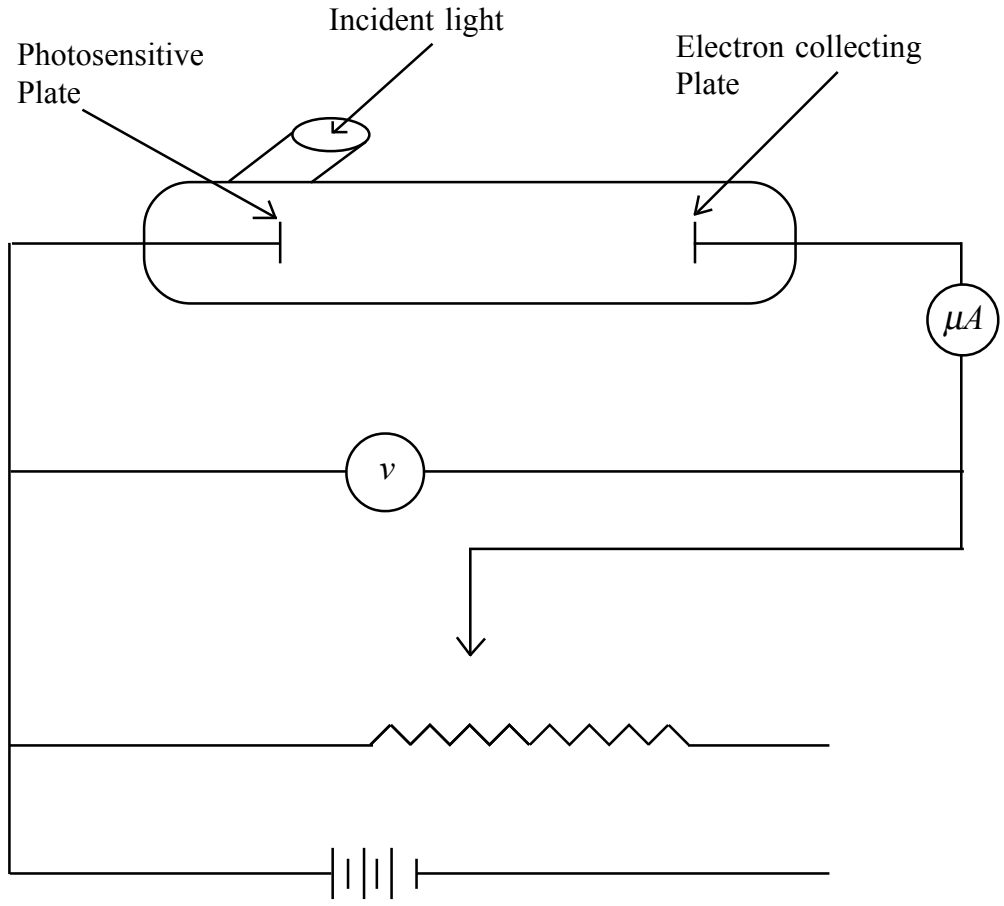


Fig. 2.2

2.4 Apparatus

Light source, light filters of different colours. Photoelectric cell, micro/milli-ammeter, voltmeter luxmeter variable voltage source.

2.5 Experimental Procedure

1. Set up the apparatus on a table so that the aperture in front of the photocell faces the light source and can be slided against it.
2. Connect a voltmeter to measure the retarding potential as shown in figure 6.2 connect a micro ammeter in series with the anode (electron collecting plate) to measure the photocurrent.
3. Turn on the equipment with the retarding voltage set to zero and no light an the photocut-mode set the "Zero Adjustment" know so that the photocurrent is nearly zero < 1.0 μA or so. Note the fluctuations in "dark current".
4. Maunt a fillter, the green one is good to start turn on the mercury lamp or other source provided to you and place it as close as possible to the filter. The current amplifier is protected so that off scale readings will not horn it. In that case, you can use miliammeter in place of micro-ammeter instead.
5. Gradually increase the retarding potential and record the corresponding photocurrent. Note the reterding potential where the current just reduces to zero.

   This is the stopping voltage or stopping potential.
6. Record current vs. retarding voltage systematically. Do the same for different incident frequencies. (colours) (i.e. for other filters).
7. Draw stopping potentials against different frequencies. It will be a straight line and the slope of that staight line given the value of we and hences.
8. Hold and LDR/Lux meter at the surace of the photocell to meansure the relative incident intensity. Vary intersity of the source gradually step by step and record the corresponding photoelectric current at a particular frequency with a given accelerating potential.
9. Draw photoelectric current at particular frequency against incident intensity observe. The straight line nature of the curve.

2.6 Experimental Results

Table 1. Recording of stopping potential.

Sl. No.	Colours	Retarding Potential in Volt	Photoelectric Current in μA
	Red	O	
		V	O
	Blue	O	
		V	O
	Yellow	O	
		V	O
	Green	O	
			O

Table 2. Data for stopping potentials vs. Frequency graph (extracted from Table 1)

Sl. No.	Colours	Wavelength (λ)	Frequency $\nu = \frac{c}{\lambda}$	Stopping Potential (v_s) in volt

Table 3. Recording of Photoelectric current for varying incident intensities for an accelerating potential = ... volt.

Sl. No.	Colours of light filter	Incident Intensity in Lux (or, LDR current in μA)	Photoelectric Current (μA)
	Red		
	Blue		
	Yellow		

	Green		

Alternative Table 3(a). If Lux meter or LDR arrangement is not available Recording of Photoelectric current for varying distance of the constant intensity source for an Accelerating potential = ... volt

Sl. No.	**Colours of light filter**	**Distance of the source from the photo cell (d) in cm**	**Value of $\frac{1}{d^2}$ cm^{-2}**	**Photoelectric current (μA)**
	Red	5		
		10		
		20		
		30		
		40		
	Blue	0		
		10		
		20		
		30		
		40		
	Yellow	5		
		10		
		20		
		30		
		40		

	Green	5		
		10		
		20		
		30		
		40		

Draw photoelectric current (i) at particular colour (frequency or war length) againsth against incident intensity. Conclude about your observation from the graph about the variation of photo electric current at particular frequency or wavelength against incident intensity. Alternatively, draw photoelectric current (i) vs $\frac{1}{d^2}$ graph.

Draw V_s versus v graph, and calculate h.

Value of h = electric charge (e) × slope of V_s versus v graph.

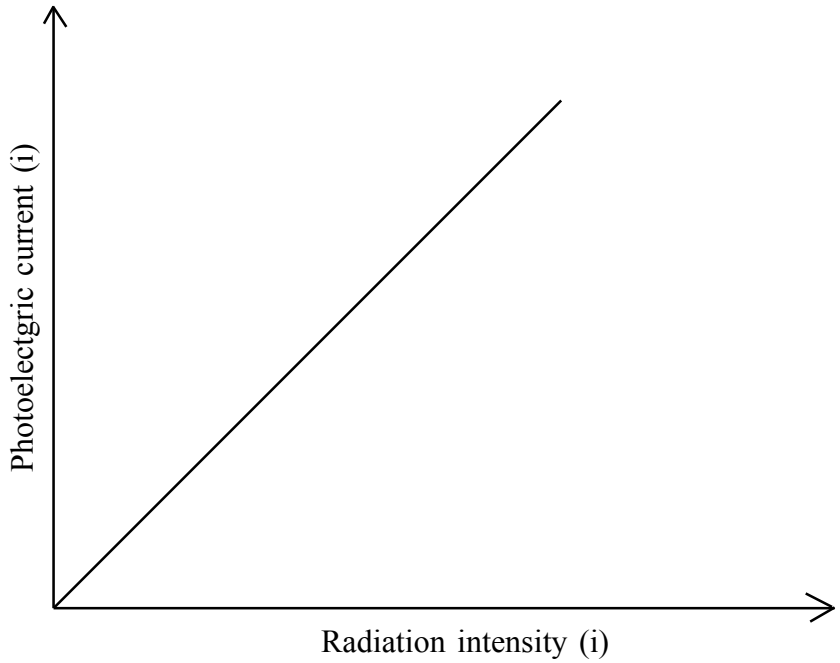


Fig. 2.3 : Variation of photoelectric current (i) with the intensity of photocell incident light

2.7 Discussion

1. The alignment of source, filter and cathode surface of the photocell should be made carefully.
2. Recording of the photoelectric current with increasing retarding potential should be made systematically to get stopping potential, otherwise exact value of retarding potential for which photoelectric current just reduces to zero may be overlooked.

2.8 Summary

- Photoelectric effect experiment showing light is also a particls Energy comes in particle like chums-basis of quantum physics.
- Based on the wave model of light, physicists predicted that increasing light amplitude would increase the kinetic energy of emitted photoelectrons, while increasing the frequency would increase measured current.
- Experiments showed that increasing the light frequency increased the kinetic energy of the photoelectrons, and increasing the light amplitude increased the current.

2.9 Exercise and Answer

1. Write down Einstein's postulates on photoelectric effect.

Ans. — See theory.

2. Write down Einstein's equation of photoelectric effect.

Ans. — See theory.

3. What is threshold frequency for photoelectric effect?

Ans. — There is a certain minimum frequency v_0 of incident radiation below which there is no emission of photoelectrons. This frequency is called the threshold frequency which depends on the material and the nature of the emitting surface.

4. What do you meant by photoelectrons?

Ans. — The metals that exhibit the photoelectric effect are called photosensitive materials and the emitted electrons are called photoelectrons.

5. What is the stopping potential or cut-off voltage?

Ans. — The negative anode voltage which just stops the most energetic photoelectrons and reduces photocurrent to zero is called stopping potential or stopping voltage or cut-off voltage.

6. Define work function for photoelectric effect?

Ans. — Work function for photoelectric effect is defined as the energy needed to remove the least fightly bound electrons from the surface of a metal.

7. Draw the graph intensity of radiation vs frequency.

Ans. — See the theory.

8. What is the significant of photoelectric effect?

Ans. — The photoelectric effect is significant because it demonstrates that light has particle like qualities. It established that we can consider light as quanta of (packets) of energy (photon) where one photon interacts with one electron and each photons must have sufficient energy to remove each electron.

Unit 3 ❑ Determination of slit width by studying the single slit diffraction pattern

Structure

3.1 Objective

Determination of slit width by studying the single slit diffraction pattern.

3.2 Introduction

When light waves face an obstacle (size is comparable to the wavelength) in its path, the waves bend round the edges. This bending of light waves is known as diffraction. There are two types of diffraction (i) Fresnel diffraction and (ii) Fraunhofer diffraction. In Fresnel diffraction, source and screen are at finite distances from the obstacle. In Fraunhofer diffraction, source and screen are at infinite distances from the obstacle.

3.3 Apparatus required

Apparatus required: Laser source, single slit, screen, photo detector, multimeter.

3.4 Theory and Formula used

A plane wavefront is incident normally on a slit of width d as shown in Fig. l. According to Huygens's principle, each point on the plane wavefront become sources of secondary wavelets. The secondary wavelets which travel in a direction parallel to the direction of incident beam make a central maximum.

The secondary wavelets which travel in a direction making an angle θ with central axis will have maximum and minimum intensity, depending upon their path difference.

Apart from central maximum, secondary maxima will form in between secondary minima on both sides of the central maximum.

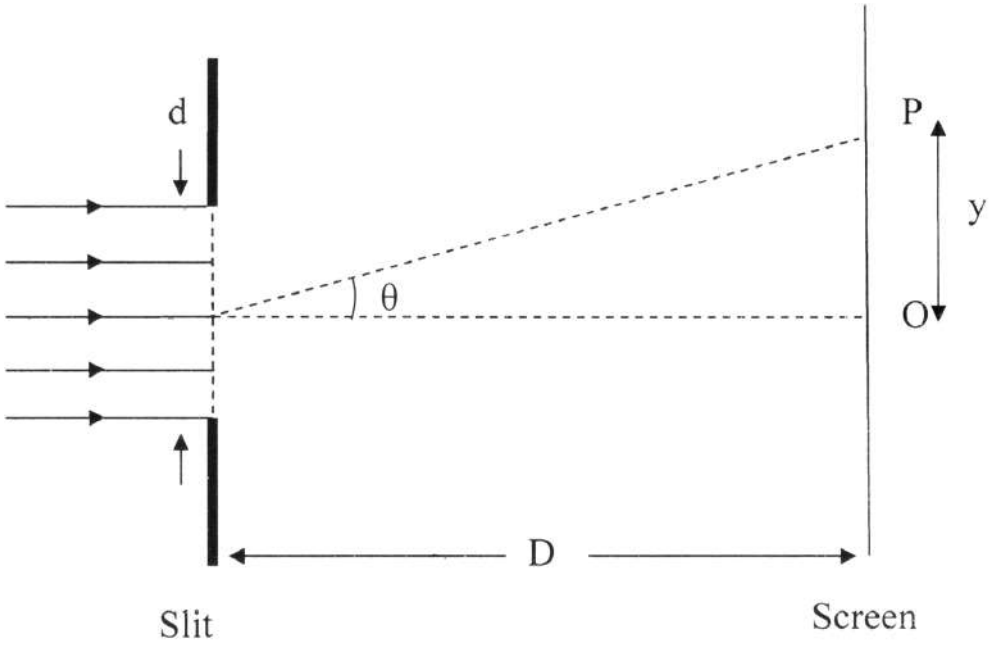


Fig. 1. Diffraction through a single slit.

If the distance of the first secondary minimum from the centre of the central maximum is y, then width of the central maximum is twice i.e. $2y$

The directions of secondary minima are given by equation

$$d \sin \theta = m\lambda \quad \text{..... (1)}$$

where d is the width of the slit, λ is the wavelength of the light, $m = \pm 1, \pm 2, \pm 3$ .....

For first minimum, $m = 1$

$$d \sin \theta = \lambda \quad \text{..... (2)}$$

For a large value of D, we can approximate sine by y/D. Thus, our equation becomes

$$d(y/D) = \lambda \quad \text{..... (3)}$$

$$y = \frac{\lambda D}{d} \quad \text{..... (4)}$$

$$\text{Width of the central maximum} = \frac{2\lambda D}{d} \quad \text{..... (5)}$$

$$\text{Slit width} \qquad d = \frac{2\lambda D}{\text{width of central maximum}} \quad \text{..... (6)}$$

3.5 Experimental Procedure

1. For emission of constant light intensity from the laser source, switch ON the laser before starting the experiment.
2. Setup the laser and make incident the beam on to the slit, keep the screen/ photo detector far behind the slit.
3. A diffraction pattern as shown in Fig. 2 will be formed behind the slit, try to observe it on a screen first and then allow to fall on the photo detector.
4. For plotting intensity profile of the diffraction pattern, a photodetector connected with a multimeter is being used.
5. Set the position of photo detector on second minima of the diffraction pattern and note down the reading of current. Now shift the photo detector with the help of translation stage towards the central maximum and take the recordings current vs position of the photo detector. Continue the shifting of the photodetector inthe same direction until second minima will come again in opposite direction.
6. Plot a graph between position of photo detector vs current. From the graph, measure the distance between two first minima on either side of central maxima, which is width of the central maxima.

7. Measure the slit and photodetector's separation and calculate the width of the slit using equation (6).
8. Repeat the above procedure.

Note: If photo detector is not available, then one can proceed by an alternative method. Using a graph paper in place of photo detector (mentioned in point number 3) where diffraction pattern will form, and marking the pattern (maxima and minima including central maximum) by a pencil, and then measuring the width of the central maximum by a scale, one can calculate slit width from the relation $d = \frac{2D\lambda}{width\ of\ central\ maximum}$, where 0 is distance between slit and graph paper.

3.6 Observation

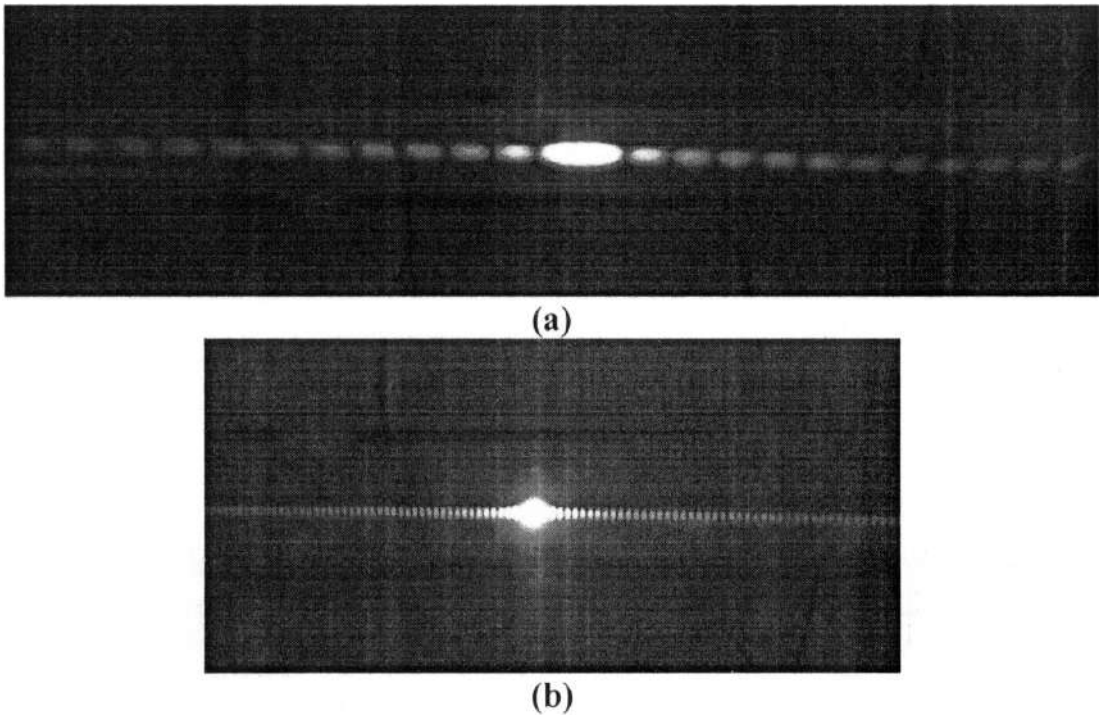


Fig. 2. (a-b) Photographs of single slit diffraction patterns of two different slit widths.

Table 1. Intensity profile data

Sl. No.	Photodetector's Position	Current value
1.		
2.		
3.		
4.		
5.		

3.7 Calculation

(i) Plot a graph between photodetector's position vs current.

(ii) From the graph, measure width of the central maximum = distance between two first minimum on either side of central maxima = ... mm

Table 2. Slit width measurement

Sl. No.	Wavelength of laser source (λ)	Distance between slit and photodetector (D)	Width of the central maximum (from graph)	Slit width $d = \frac{2\lambda D}{width\ of\ central\ maximum}$
1.				
2.				
3.				
4.				
5.				

Mean slit width = ... /μm

3.8 Precautions

1. Never keep your eyes in the path of the laser beam.
2. Laser should be switched ON before starting the experiment.

3. Photo detector should be far away from the slit.
4. Translation stage should be move gradually.

3.9 Oral Questions

1. What is diffraction?
2. What is the basic difference between interference and diffraction phenomena?
3. What are two types of diffraction, mention the differences between them?
4. Give an example which can be explained by diffraction phenomenon.

Unit 4 ❑ Use of an OPAMP as adder, subtractor, invering and non-inverting amplifier

Structure

4.1 Objective

Use of an OPAMP as adder, subtractor, inverting and non-inverting amplifier.

4.2 Introduction

Operational amplifier (OPAMP) is a direct coupled high gain differential amplifier. It is basically used to compute mathematical functions like addition, subtraction, integration, differentiation etc.

An ideal OPAMP has some important characteristics like infinite voltage gain, infinite input impedance, zero output impedance, infinite bandwidth, characteristics is independent of temperature and perfect balance.

Pin diagram of IC 741 is shown in Fig. 1. It has two input terminals and one output terminal. Terminal marked with (+) is non-inverting input terminal and marked with (–) is inverting input terminal.

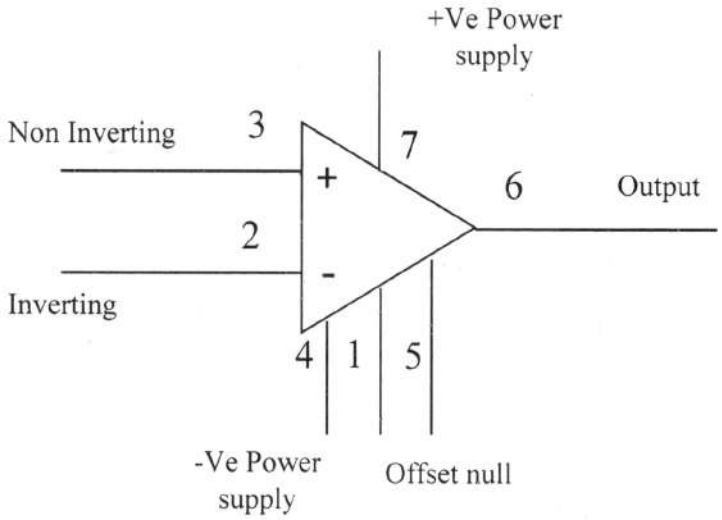


Fig. 1. Pin diagram of IC 741.

4.3 Apparatus required

IC OPAMP 741, DC power supply, Function generator, Digital storage oscilloscope, Resistances, Connecting wires.

4.4 Adder or Summing Amplifier

Op-amp is used to design a adder circuit or summing amplifier whose output is the sum of input signals. Schematic of the circuit diagram of adder or summing amplifier is shown in Fig. 2.

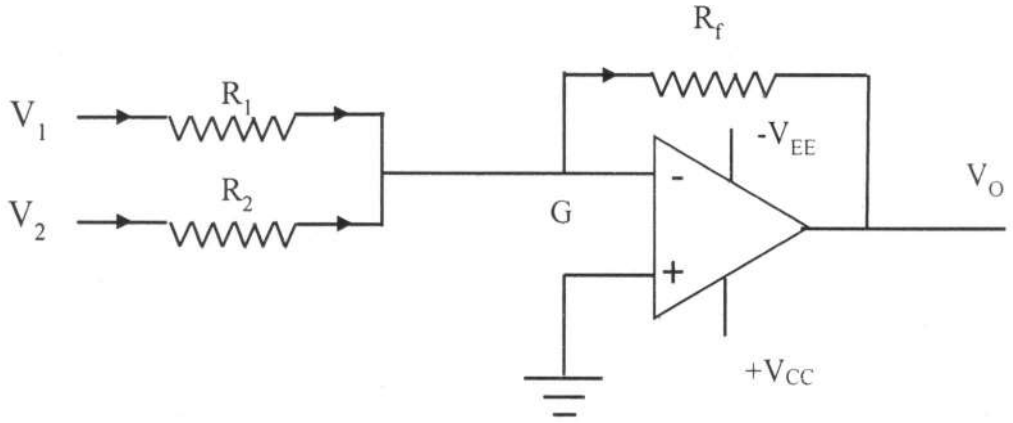


Fig. 2. Circuit diagram of Adder or summing amplifier.

$$\frac{V_1}{R_1}+\frac{V_2}{R_2}=-\frac{V_0}{R_f} \tag{1}$$

$$V_0=-\left(\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2\right)$$

If $R_1 = R_2 = R$

$$V_0=-\frac{R_f}{R}(V_1+V_2)$$

For $R_f = R$

$$V_0 = -(V_1 + V_2) \tag{2}$$

Output voltage is equal to sum of input voltages V_1 and V_2.

Procedure

1. Setup the circuit as per diagram shown in Fig. 2.
2. Connect the +ve and -ve supply voltages to pin number 7 and 4.
3. Apply voltages V_1 and V_2 to the input terminals.
4. Vary the input voltages and note down the corresponding output voltages in table 1.

Table 1

Input Voltage		**Output Voltage**
V_1	V_2	V_0

4.5 Differential Amplifier or Subtractor

Schematic of the circuit diagram of Differential Amplifier or Subtractor is shown in Fig. 3.

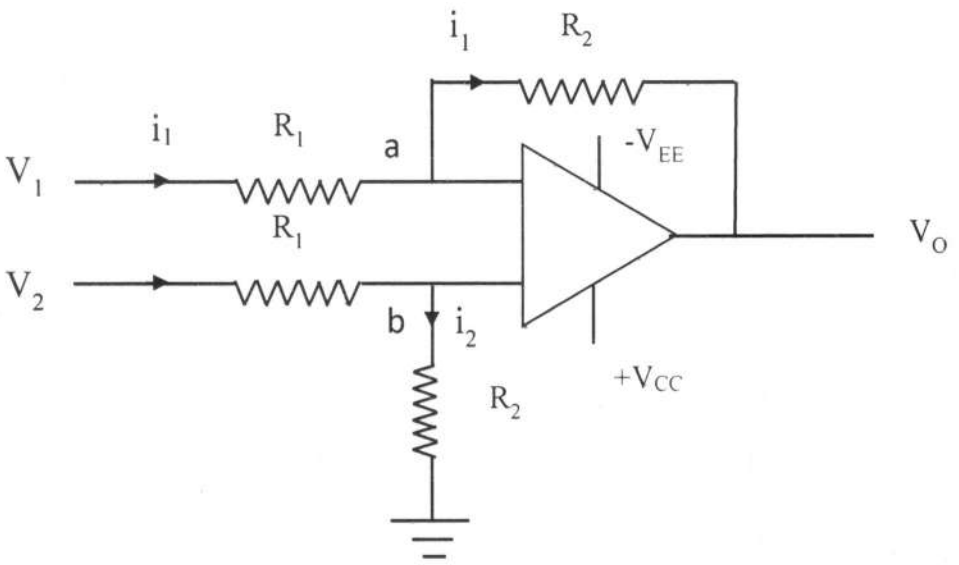


Fig. 3. Circuit diagram of Differential Amplifier or Subtractor circuit.

Potential at point *a* and *b* is V_x

$$\frac{V_1 - V_x}{R_1} = \frac{V_x - V_0}{R_2} \tag{3}$$

$$\frac{V_2 - V_x}{R_1} = \frac{V_x}{R_2} \tag{4}$$

Subtracting equation (3) and (4)

$$V_0 = \frac{R_2}{R_1}(V_2 - V_1) \tag{5}$$

Output voltage is amplified version of the difference of input voltages V_2 and V_1.

Procedure

1. Setup the circuit as per diagram shown in Fig. 3.
2. Connect the +ve and –ve supply voltages to pin number 7 and 4.

3. Apply the voltages V_1 and V_2 to the input terminals.
4. Vary the input voltages and note down the corresponding output voltages in table 2.

Table 2

Input Voltage		**Output Voltage**
V_1	V_2	V_0

4.6 Inverting Amplifier

Schematic of circuit diagram of inverting amplifier using OPAMP is shown in Fig. 4.

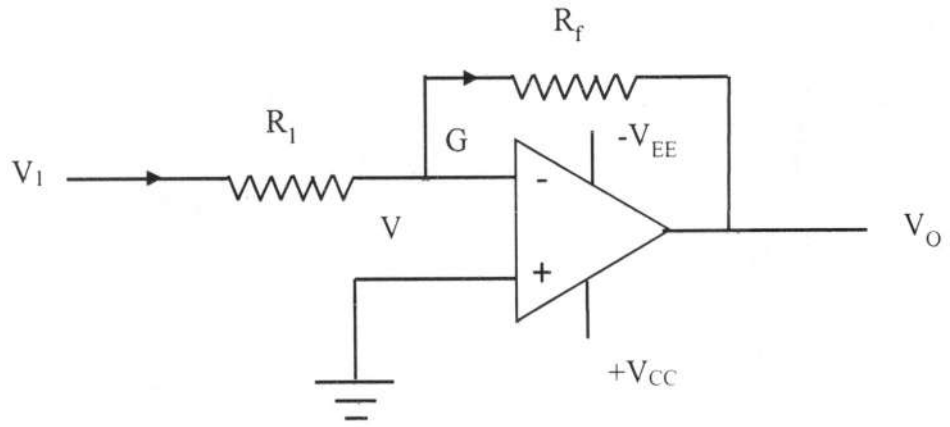


Fig. 4. Circuit diagram ofInverting Amplifier.

Applying Kirchhoffs current law at the point G gives

$$\frac{V_1 - V}{R_1} = \frac{V - V_0}{R_f} \tag{6}$$

As the point G is a virtual ground, $V \approx 0$

$$\frac{V_1}{R_1} = -\frac{V_0}{R_f}$$

$$V_0 = -V_1 \frac{R_f}{R_1} \tag{7}$$

$$A_f = \frac{V_0}{V_1} = -\frac{R_f}{R_1} \tag{8}$$

Voltage gain Ar is called the closed loop gain, the negative sign shows that output voltage is 180° out of phase with respect to the input voltage.

PROCEDURE

1. Setup the circuit as per diagram shown in Fig. 4.
2. Connect the +ve and –ve supply voltages to pin number 7 and 4.
3. Apply input voltage to the inverting terminal from a function generator.
4. Measure corresponding output voltages and hence calculate the gain.

Table 3

Input Frequency (Hz)	Input Voltage (V_i)	Output Voltage (V_o)	Gain = (V_o/V_i) (Practical)	Gain = –(R_f/R_1) (Theoretical)

4.7 Non-inverting Amplifier

Schematic of circuit diagram of non-inverting amplifier using OPAMP is shown in Figure 5.

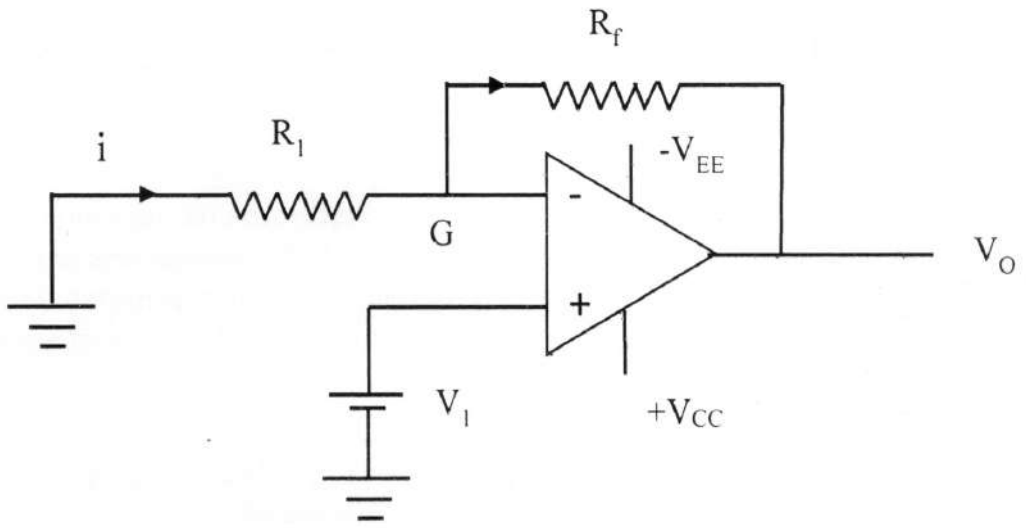


Fig. 5. Circuit diagram of Non-inverting Amplifier.

$$V_0 = V_1\left(1+\frac{R_f}{R_1}\right) \tag{9}$$

$$A_f = \frac{V_0}{V_1} = 1+\frac{R_f}{R_1} \tag{10}$$

A_f is called voltage gain of the amplifier, which is greater than 1 by a factor $\left(\frac{R_f}{R_1}\right)$. There is no phase difference between input voltage and output voltage.

PROCEDURE

1. Setup the circuit as per diagram shown in Fig. 5.
2. Connect the +ve and –ve supply voltages to pin number 7 and 4.
3. Apply input voltage to the non-inverting terminal from a function generator.
4. Measure corresponding output voltages and hence calculate the gain.

Table 4

Input Frequency (Hz)	Input Voltage (V_i)	Output Voltage (V_o)	Gain = (V_o/V_i) (Practical)	Gain = 1+(R_f/R_1) (Theoretical)

4.8 Precautions

1. Connections should be verified before switch ON the instrument.
2. Input voltage should remain constant during the period of observation.

4.9 Oral Questions

1. What is an operational amplifier?
2. What are the applications of OPAMP?
3. How many output terminals are there in OPAMP?
4. What is the function of inverting terminal?

Unit 5 ❑ To test a transistor using multimeter. To design a switch (NOT gate) using a transistor & study its performance

Structure

5.1 Objective

To test a transistor using a multi meter. To design a switch (NOT gate) using a transistor and study its performance.

5.2 Introduction

A bipolar junction transistor (BJT) consists of two pn junctions. Transistors have three terminals-emitter, base and collector. The emitter is highly doped, base is lightly doped and collector is moderately doped. BJTs are of two types npn and pnp.

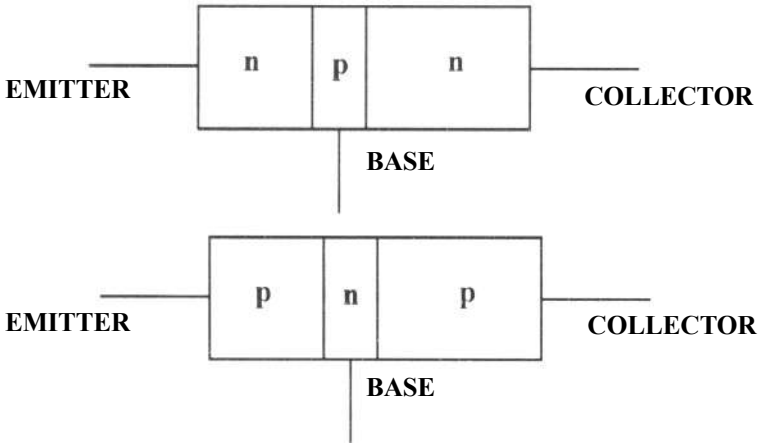


Fig. 1. (a) npn transistor (b) pnp transistor

5.3 Apparatus required

Transistor, multimeter, resistors.

A. Transistor testing

Transistor testing is carried out by applying the concept of pn-junction biasing. When a forward bias is applied to the pn-junction the junction allows current to pass through it and when reverse bias, it behaves as an open circuit. we can identify a transistor whether it is NoPN or PNP by testing the junction's continuity in the forward biasing mode and reverse biasing mode.

Experimental Procedure

First of all, set the knob of digital multimeter to Diode/Continuity position.

Testing of NPN Transistor

(i) Connect the positive probe of multimeter to the base terminal of the transistor and negative or common probe to the either emitter terminal or collector terminal (as shown in Fig. 2). In both the cases forward biasing condition will satisfy and multimeter will show some reading.

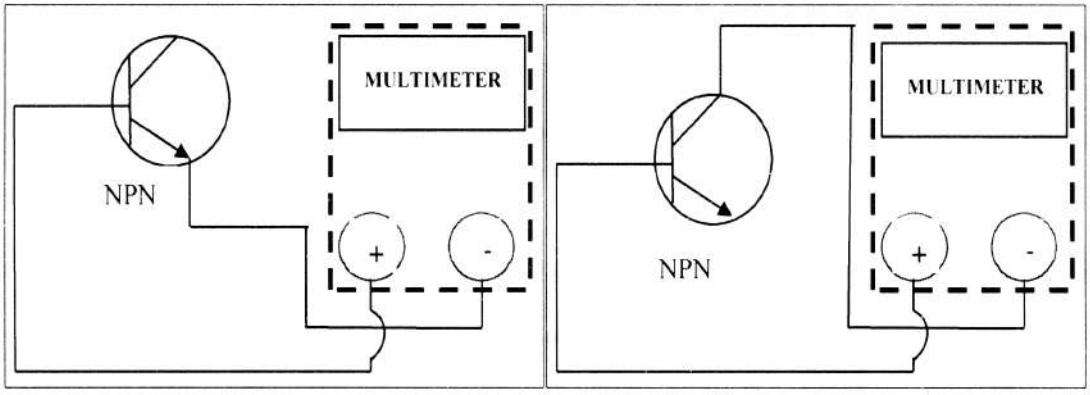


Fig. 2

(ii) Connect the negative probe of multimeter to the base terminal of the transistor and positive probe to either emitter terminal or collector terminal (as shown in Fig. 3). In both the cases reverse biasing condition will satisfy and multi meter will show open circuit condition.

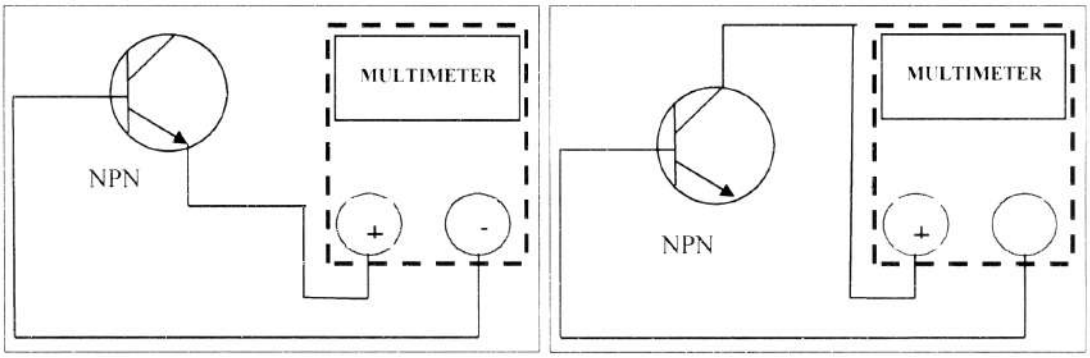


Fig. 3

(iii) Connect the negative probe of multi meter to the emitter and the positive probe to the collector. The multimeter will show open circuit condition. After interchanging, the positive probe to emitter and the negative probe to the collector (as shown in Fig. 4), still multi meter will show open circuit condition. Multimeter will show an open circuit condition between emitter and collector for both the directions.

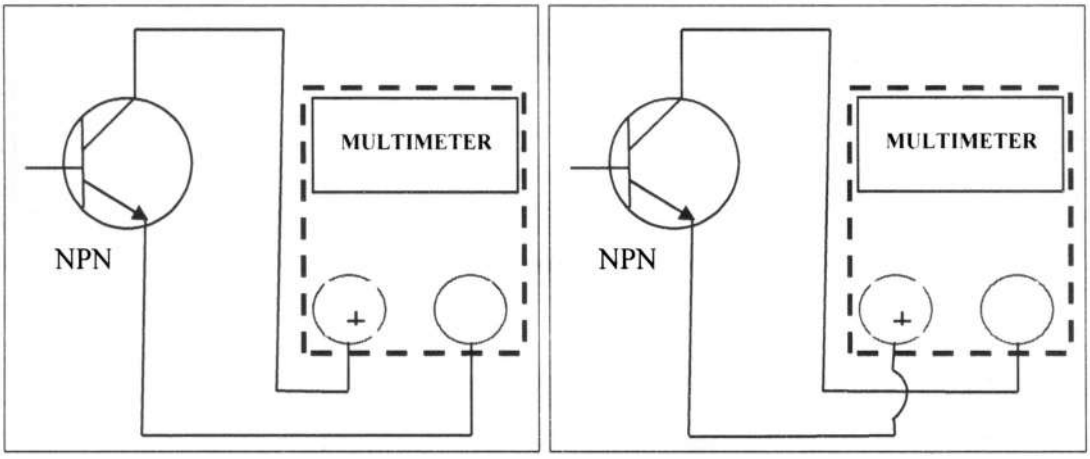


Fig. 4

Testing of PNP Transistor

(i) Connect the negative probe of multimeter to the base terminal of the transistor and positive probe to either emitter terminal or collector terminal (as shown in Fig. 5). In both the cases forward biasing condition will satisfy and multimeter will show some reading.

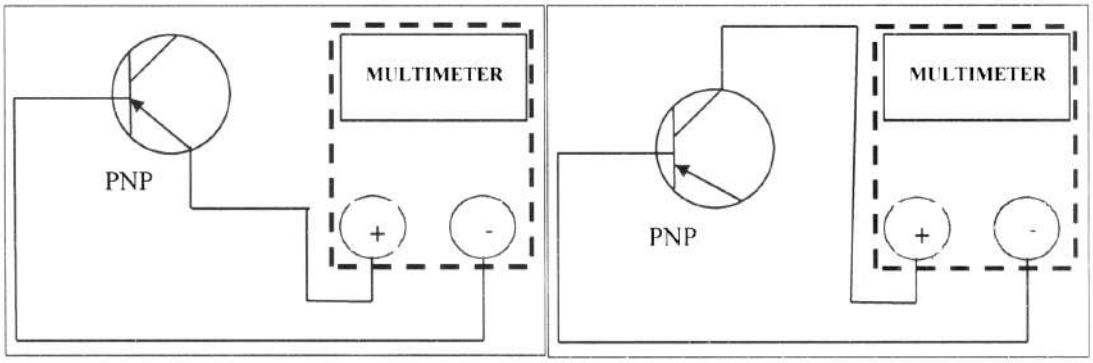


Fig. 5

(ii) Connect the positive probe of multimeter to the base terminal of the transistor and negative probe of multi meter to either emitter terminal or collector terminal (as shown in Fig. 6). In both the cases reverse biasing condition will satisfy and multimeter will show open circuit condition.

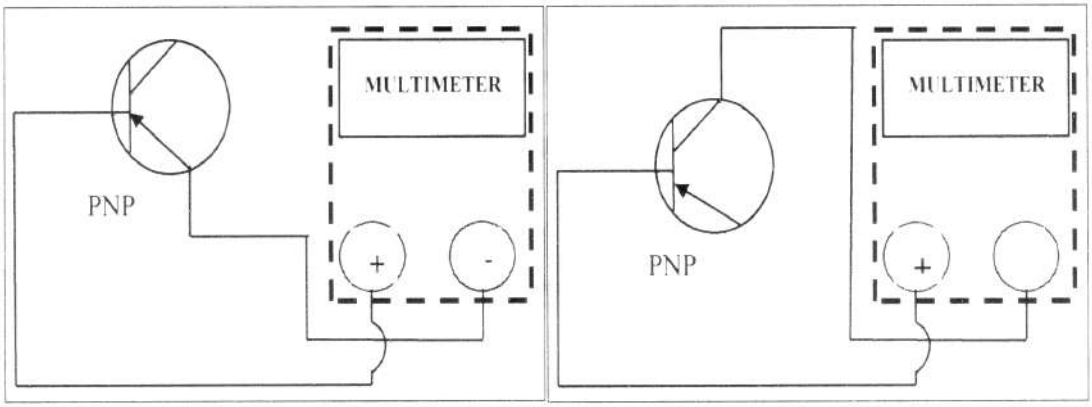


Fig. 6

(iii) Connect the negative probe of multi meter to the emitter and the positive probe to the collector. The multimeter will show open circuit condition. After interchanging, the positive probe to emitter and the negative probe to the collector (as shown in Fig. 7), multimeter will show open circuit condition. Multimeter will show an open circuit condition between emitter and collector for both the directions.

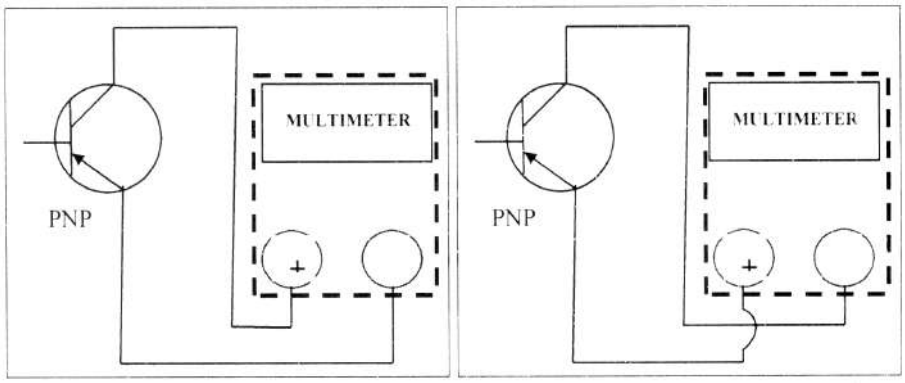


Fig. 7

B. Design of switch (NOT gate) using transistor

A NOT gate is called inverter because it inverts the input. For high input, output will be low and for low input, output will be high. A switch or NOT gate can be realized using a transistor.

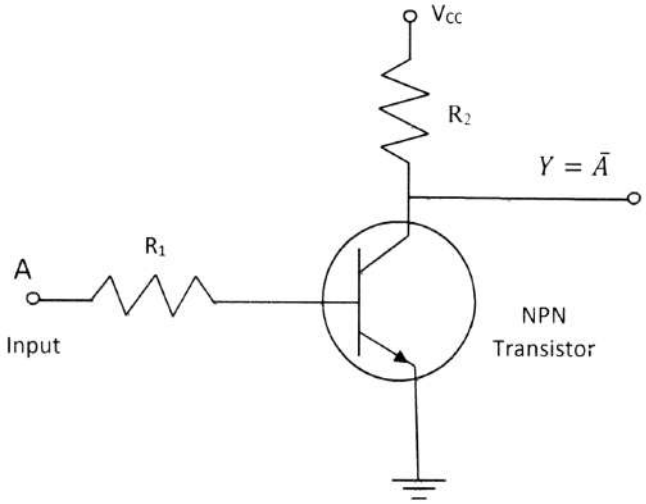


Fig. 8. NOT Gate using a Transistor

5.4 Experimental Procedure

(i) At first connect the circuit as per diagram shown in Fig. 8.

(ii) When high voltage is applied as input to terminal A of the transistor. Transistor move to ON state. When the transistor is in ON state, transistor

behaves like short-circuited, so the voltage V cc gets dropped at R_2 and no voltage appears at the output terminal which is in logic low.

(iii) When low voltage is applied as input to terminal A of the transistor. Transistor moves to OFF state. When the transistor is in OFF state, supply voltage has no path to move, entire voltage Vcc will appear at the output terminal Y which means that the output is at logic high.

Table 1. Truth table for NOT Gate

Input	**Output**
High	Low
Low	High

5.5 Precautions

1. Choose the leads of the transistor carefully.
2. Connect the circuit components properly.

5.6 Oral Questions

1. Draw the logic symbol of NOT gate.
2. Give the truth table of A NOT gate.
3. Why the emitter of transistor doped heavily compared to others?

Unit 6 ❑ To verify and design AND, OR, NOT and XOR gate using NAND gates

Structure

6.1 Objective

To verify and design AND, OR, NOT and XOR gate using NAND gates.

6.2 Introduction

The NAND and NOR gates are said to be universal gates, because realization of other logic gates with the help of NAND and NOR gates are possible. le 7400 consist of four NAND gates. Each NAND gate utilizes two input pins and one output pin. This le has fourteen pins including one power supply and one ground pin. Schematic of the pin diagram is shown in Fig. 1.

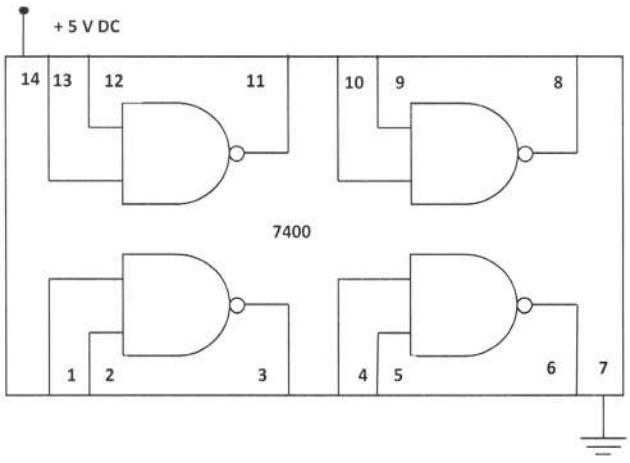


Fig. 1. le 7400 pin diagram.

6.3 Apparatus required

IC 7400, trainer kit, wires, probes, etc.

Experimental Procedure

1. Insert IC 7400 to the IC base of trainer kit and connect positive supply and ground to the pin 14 and 7 respectively.

2. Make connections of the circuit as per diagram shown in Fig. 2, Fig. 3, Fig. 4 and Fig. 5.

3. Provide various combinations of inputs to the input terminals and note down the corresponding output from the output LEDs in

4. Verify the Truth Table (Table 1, Table 2, Table 3 and Table 4).

(i) AND gate from NAND gate: If the output of one NAND gate is inverted by another NAND gate, the final output will be an AND gate.

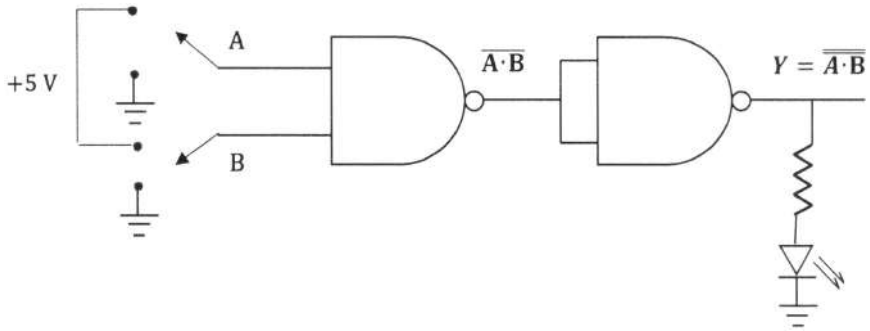


Fig. 2. Realization of AND gate using NAND gate.

$$Y = \overline{\overline{A \cdot B}}$$

$$Y = A \cdot B$$

Observation

Table 1. Truth Table of NAND Gate

INPUT		OUTPUT
A	**B**	**Y**
0	**0**	**0**
0	**1**	**0**
1	**0**	**0**
1	**1**	**1**

(ii) OR gate from NAND gate: If the output of two NOT gates realized by NAND gates are connected to another NAND gate, the final output will be an OR gate.

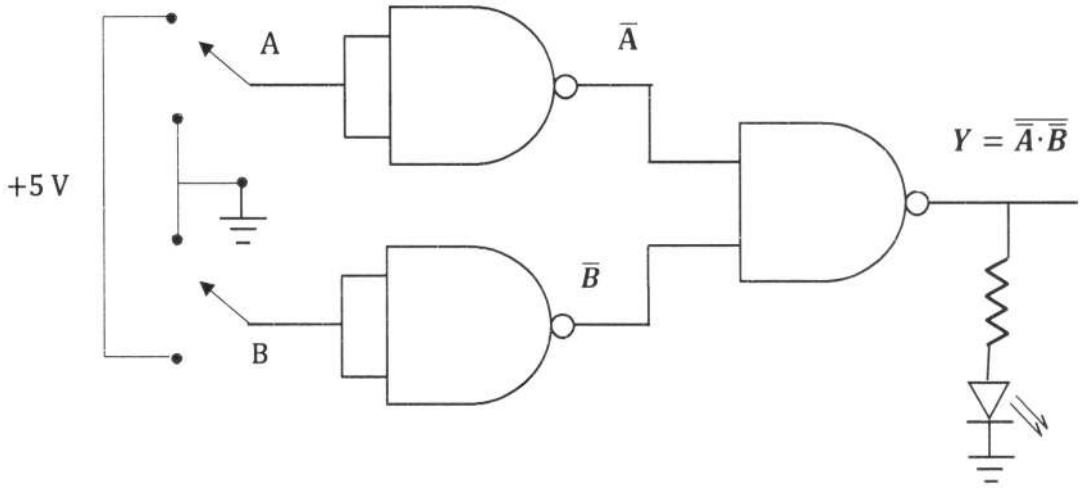


Fig. 3. Realization of OR gate using NAND gate.

$$Y = \overline{\overline{A \cdot B}}$$
$$Y = \overline{\overline{A}} + \overline{\overline{B}}$$
$$Y = A + B$$

Observation

Table 2. Truth Table of OR Gate

INPUT		OUTPUT
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**1**

(iii) NOT gate from NAND gate: If all the inputs of a NAND gates are connected together, the output will be NOT gate.

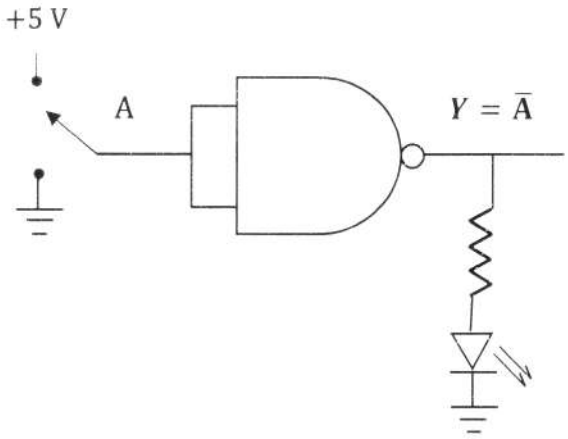


Fig. 4. Realization of NOT gate using NAND gate.

Observation

Table 3. Truth Table of NOT Gate

INPUT	OUTPUT
A	Y
0	1
1	0

(iv) XOR gate from NAND gate:

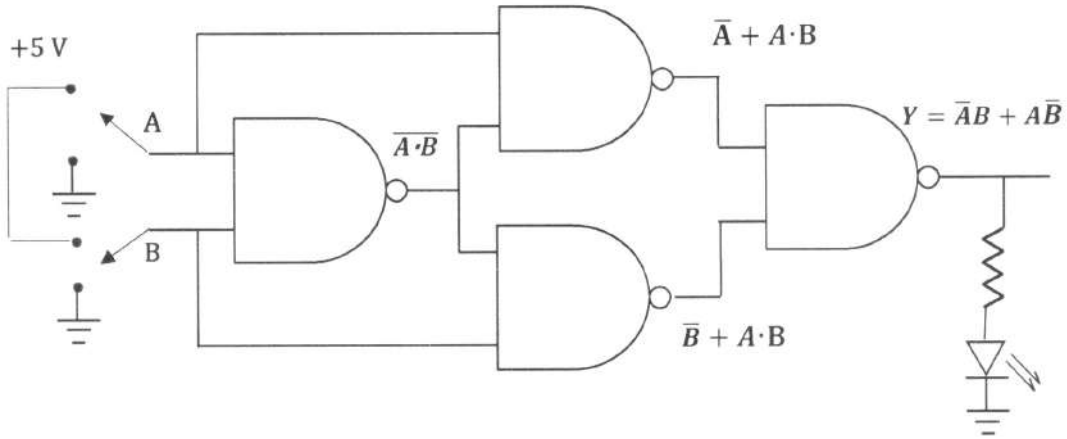


Fig. 5. Realization of XOR gate using NAND gate.

Observation

Table 4. Truth Table of XOR Gate

INPUT		OUTPUT
A	**B**	$Y = \overline{A}B + A\overline{B}$
0	**0**	**0**
1	**0**	**1**
0	**1**	**1**
1	**1**	**0**

6.4 Result

AND, OR, NOT and XOR gates are realized using NAND gates.

Truth table for these gates are verified.

6.5 Precautions

1. IC should be tested before performing the experiment.
2. Connections should be tight.

6.6 Oral Questions

1. Why NAND and NOR gates are called universal gates?
2. Realize NOR gate using minimum number of AND gates.
3. Give the truth table of XNOR Gate.

Unit 7 ❑ To design a combinational logic system for a specified Truth Table

Structure

7.1 Objective

Students can solve any logical Boolean expression by making combinational logic system, also can simplify a logical expression.

7.2 Introduction

The truth table displays the logical operations on input signals in a table format. Every Boolean expression can be viewed as a truth table. The truth table identifies all possible inputs combinations and the outputs for each. It is common to create the table so that the input combinations produce an unsigned binary up count. A combinational logic gate can specified a truth table. For a given Boolen expression, we can make a combinational logic circuit.

7.3 Theory

Problem 1 : Verify the logic identify :

$\mathbf{AB + AC + B\overline{C} = AC + B\overline{C}}$

7.3(1) 0 Theory : The logic circuit required for the verification of the logic identity AB + AC + B$\overline{C}$ = AC + B$\overline{C}$ is shown in Fig. 7.4-1. The outputs y_1 and y_2 are to be measured for all possible values ('0' and '1') of A, B and C. It is found that $y_1 - y_2$ for all possible combination of A, B and C then the identify will be verified.

7.4(1) 0 Procedure : i) At first construct the logic circuit of Fig. 7.4-1 on a bread

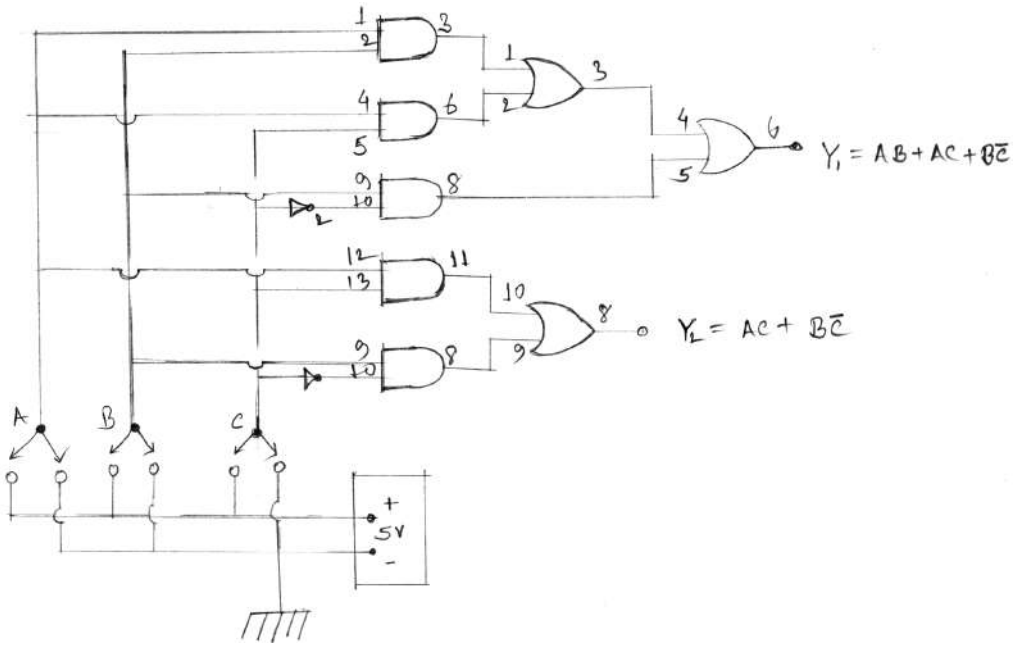


Fig. 7.4-1

board by wing ICs-7432, 7408/7409, 7404, a 5V regulated power suppy and logic switch units. Indicate the pin number used. One such possible pin number are indicated in Fig. 7.4-1. For conveniences insert the ICs with the Pins 1-7 on one side and Pins 8-14 on the other side of the central groove on the bread board connect the +ve and –ve terminals of the 5V supplying to two side lines of the bread board, which may be called '+5V live' and 'ground live'. Connect pins 14 of all ICs to this +5V live and pins 7 to ground line.

ii) Now, measure the voltage at the points A, B, C, y_1 and y_2 for all possible comibination of input voltages at A, B and C by using a dc voltmeter (0-5V). Record all these voltages in a table.

iii) Detive suitable voltage ranges '0' and '1' and obtain the truth table show that $y_1 - y_2$ for all possible input combinations.

● **Experimental data :**

Types of IC Used :

IC – 7432 (Quad 2 input AND)

IC – 740817409 (Quad 2-input AND)

IC – 7404 (Hex inverter)

(A) Data for input and output voltages to verify the identify

Table I

Input Voltages in V at			Output Voltage in V at	
A	**B**	**C**	y_1	y_2
0.0	0.0	0.0	...	...
5.0	0.0	0.0	...	...
0.0	5.0	0.0	...	...
0.0	0.0	5.0	...	...
5.0	5.0	0.0	...	...
0.0	5.0	5.0	...	...
5.0	0.0	5.0	...	...
5.0	5.0	5.0	...	...

(B) Truth table as obtained from TABLE I :

Detive 0.0 – 0.8 V as '0' and 3.0 – 5.0 V as '1'

Table II

Row	Input			Output	
	A	**B**	**C**	y_1	y_2
1	0	0	0	0	0
2	1	0	0	0	0
3	0	1	0	1	1
4	0	0	1	0	0
5	1	1	0	1	1
6	0	1	1	0	0
7	1	0	1	1	1
8	1	1	1	1	1

Note : Following the above procedure you can verify any other logic identity set in the examination. Further examples for practice.

(a) $AB + \bar{A}C = (A + C)(\bar{A} + B)$

(b) $(A + B)(A + C) = A + BC$

(c) $(A + B)(B + C)(C + A) = AB + BC + CA$

■ **Problem (2) :** A truth table is given. Write down the Boolean expression and construct a logic circuit to realize the truth table.

● **Theory :** Suppose the following is the given truth table :

A	B	y_1	y_2
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Corresponding Boolean expression can be obtained by 'the sum of the fundamental products' that produce 1 outputs. To get the output 1 for the input A = 0 and B = 1, we require the fundemental product $\bar{A}B$. Thus.

$$y_1 = \bar{A}B + A\bar{B}$$

$$y_2 = AB$$

The logic circuit implementing the Boolean expression (7.4-1) and (7.4-2) is shown in Fig. 7.4-2

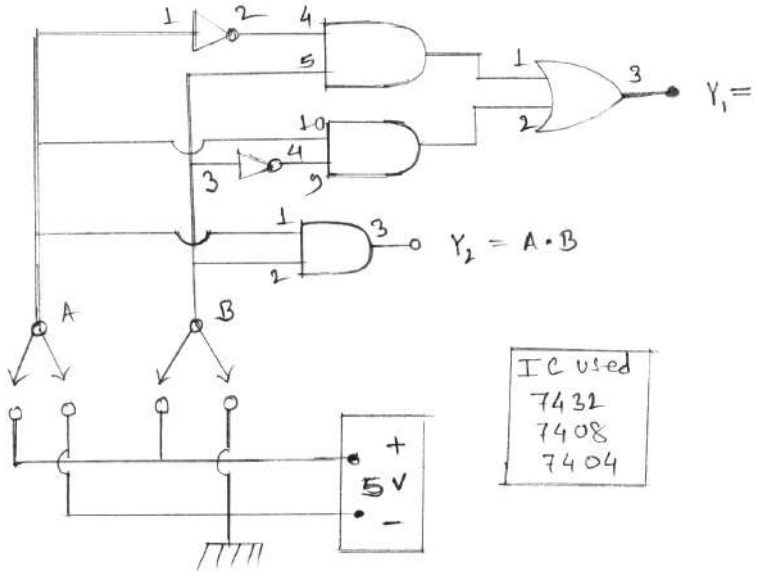


Fig. 7.4-2

● **Procidure :** (i) Construct the logic circuit of Fig. 7.4-2 on a bread board in operation (i) of problem (1).

(ii) Measure the voltages at A, B, y_1 and y_2 for all possible input combinations. Record the voltages in a table.

(iii) Define suitable voltage ranges as '0' and '1' and obtain the given truth table.

● **Experimental data :**

Types of IC used : IC – 7432
IC – 7408
IC – 7404

(A) Data for input and output voltages :

Table I

Input voltages in V at		**Output voltages in V at**	
A	**B**	y_1	y_2
0.0	0.0	...	...
5.0	0.0	...	...
0.0	5.0	...	...
5.0	5.0	...	...

(B) Truth table as obtained from Table I :

Define ..... to ..... as '0' and ..... to ..... as '1'

Table II

Input voltages in V at		**Output voltages in V at**	
A	**B**	y_1	y_2
0.0	0.0	...	...
5.0	0.0	...	...
0.0	5.0	...	...
5.0	5.0	...	...

Note : Following the procedure as describe above you can obtain the Boolean expression corresponding to any given truth table. Then you can construct the logic circuit and finally by measuring input the output voltages the given truth table can be verified. However, the following points are note worthy for consideration.

(a) The 'sum-of-products' from may be more complen than necessary. In that case, simplify the Boolean expression by wing postulates before implementing the logic circuit.

(b) Sometimes an alternative 'products-of-sums' form may come out to be convenient. For example, consider the truth table of OR gate :

A	**B**	***y***
0	0	0
1	0	1
0	1	1
1	1	1

In the 'sum-of-products' form the logic function is,

$Y = A\bar{B} + \bar{A}B + AB$

Here one considers those rows for which $y = 1$; it a variable has the value 0 it is complemented and it the variable has the value 1 it is left unchanged.

$Y = A(\bar{B} + B) + \bar{A}B$

$= A + \bar{A}B$

$= A(1 + B) + \bar{A}B$

$= A + (A + \bar{A})B$

$= A + B$

But in the 'product-of-sums' form the logic function is obtained at once as $y = A + B$. Here one considers only those rows for which $y = 0$; if a variable has the value 0 it is left unchanged and it the variable has the value 1 it is complemented.

■ **Problem (2) : Implement the logic circuit of an equality detector which gives an output 1 if A and B are both 1 or both 0.**

7.3(ii) ● Theory : The truth table corresponding to the given problem is the following :

A	**B**	***y***
0	0	1
1	0	0
0	1	0
1	1	1

The 'sum-of-product' form of the Boolean expression is

$$Y = \overline{A} \cdot \overline{B} + AB$$

The logic circuit implementing this Boolean expression is shown in Fig. 7.4-3.

7.4 Apparatus

7.4(ii) ● Procedure and Experimental data :

[Similar to that in problem (2)]

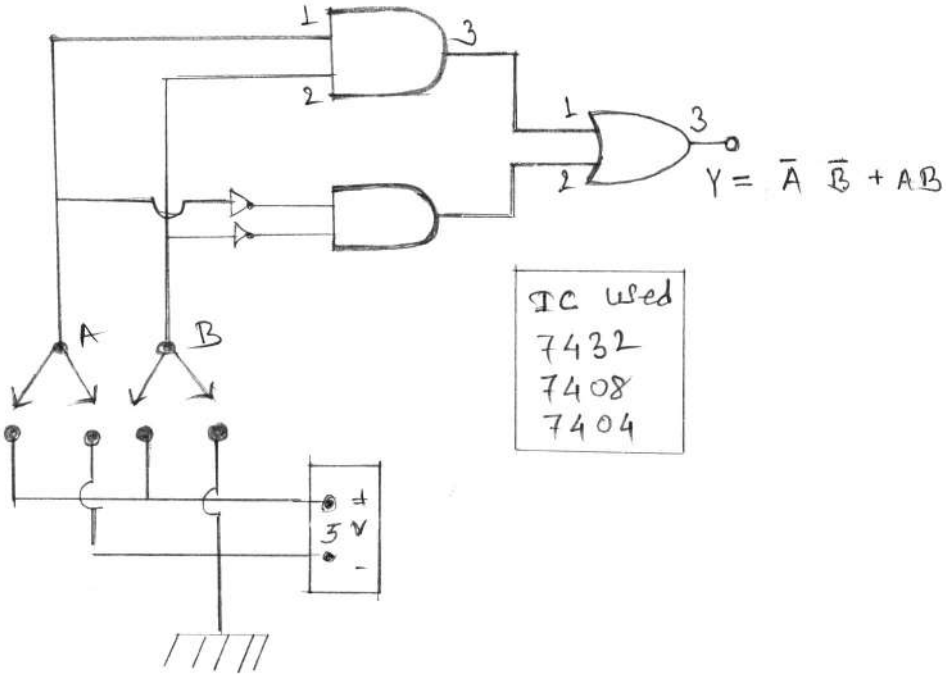


Fig. 7.4-3

7.8 Summary

A truth table is a mathematical table used in logic specially in connection with Boolean Algebra, boolean functions and propositional calculus which sets out the functional values of logical expressions on each of their functional arguments i.e. for each combination of values taken by their logical variables. In particular, truth tables can be used to show wether a propositiona expression is true for all legititime input values, i.e. logically valid.

7.9 Exercise and Answer

★ **What is a truth table?**

➢ Instead of describing in words the input-output relationship of a logic gate for all possible input combinations can be shown in a table. This table is known as truth table.

★ **What is a LED?**

➢ LED stands for light emitling diode. It is a special type of semiconductor diode made of direct gap semiconductors like GaAs. It emits light in forward biased condition due to recombination of holes and electron. In Si and Ge recombination occured via traps so, the energy liberated is converted into heat. But in GoAs, direct recombination leval place without the aid of traps and hence the energy released appears in the form of light.

★ **What are the practical used of the basic logic gated?**

➢ They are the basic 'building blocks' of more complex digital circuits including a digital computer.

★ **What do you use a resistor in series with the LED?**

➢ To limit the current through the LED to the safety limit (typical current rating is at the order of 50 mA).

★ **What is an inverter?**

➢ Since a NOT circuit inverts the sense of the output with respect to the input, the circuit is also called an inverter.

★ **In a NOT circuit what condition of a transistor indicate a logical 1 and a logical 0 state?**

➢ When the transistar is in cutoff the output is high i.e., a logical 1 state. When the transistor is in sathration, the output is low i.e. a logical 0 state.

★ **Can you identify the material of the transistar from the given data?**

➢ Yes, it V_{BE} = 0.7 V then it is Si-made, it $V_{BE} \approx$ 0.3 V then it is Ge-made.

Unit 8 ❑ To design Half Adder. Full Adder using ICs

Structure

8.1 Objective

To design Half Adder and Full Adder using ICs.

8.2 Introduction

In the combinational circuits, different logic gates are used to design encoder, multiplexer, decoder and de-multiplexer. These circuits have some characteristics, like output of this circuit, mainly depends on the levels which are there at input terminals at any time. This circuit does not have any influence on the current state. The inputs and outputs of a combinational circuit are 'n' no. of inputs and 'm' no. of circuits are half adder and full adder, substractor, encoder, decoder, and multiplexer.

8.3 Theory

A half-adder is a logic circuit which can add two binary digits and provides a sum (S) and a carry (C). The truth table of a half-adder is shown in table A. From the truth table we obtain the Boolean expressions for S and C as

$S = \bar{A}B + A\bar{B}$

and $C = AB$

Table A

Input		Output	
A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The circuit realization of a half-adder using basic gates is shown in Fig. 8(i).

A full-adder is a logic circuit which can add three binary digits at a time giving a sum and a carry. The truth table of a full-adder is shown in table B, where A_n and B_n are the n-th order bits of two binary numbers to be added and C_{n-1} is the carry generated from the of the lower $(n - 1)$th order bits. From the table we get the Boolean expressions S_n and C_n as

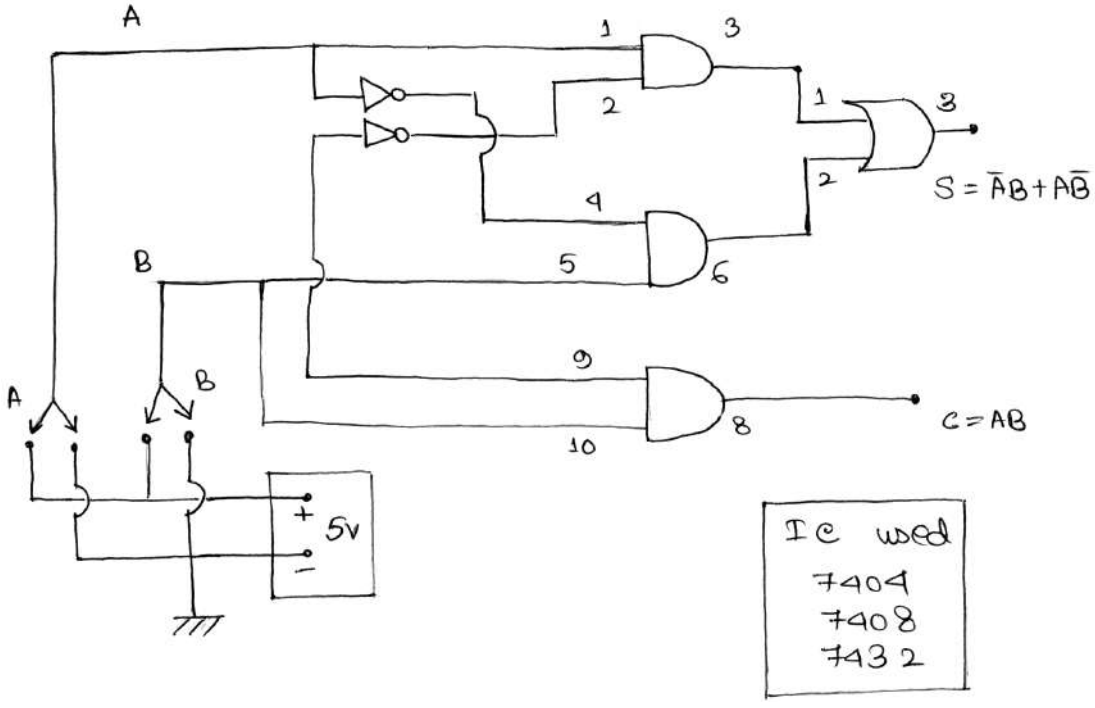


Fig. 8(i)

$$S_n = \overline{A}_n \overline{B}_n C_{n-1} + \overline{A}_n B_n \overline{C}_{n-1} + A_n \overline{B}_n \overline{C}_{n-1} + A_n B_n C_{n-1}$$

$$C_n = \overline{A}_n B_n C_{n-1} + A_n \overline{B}_n C_{n-1} + A_n B_n \overline{C}_{n-1} + A_n B_n C_{n-1}$$

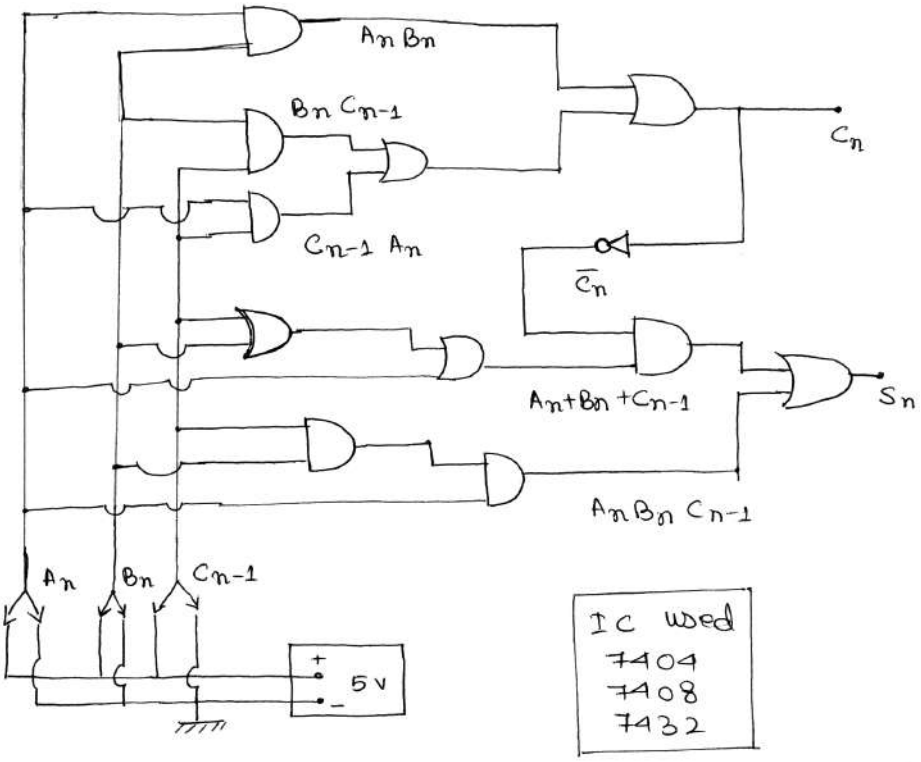


Fig. 8(ii)

Table B

Input			Output	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Using Boolean postulates these expressions can be simplified to

$$S_n = (A_n + B_n + C_{n-1})\ \overline{C}_n + A_n B_n\ C_{n-1}$$

and $C_n = A_n\ B_n + B_n\ C_{n-1} + C_{n-1}\ A_n$

The logic circuit implementing these Bodean expressions using basic gates is shown in Fig. 7.5-2.

8.4 Apparatus

(i) IC-7432, IC-74087409, IC-7404, IC-7400, IC-7402, (ii) a regulated dc power supply (5V, 1A), (iii) a dc voltmeter (0-5V) or a digital multimeter, (iv) a bread board, some single strand wires and logic switch (SPDT) units.

8.5 Experimental Procedure

(i) At first construct the logic circuit of Fig. 7.5-1 on a breed board by using ICs 7404, 7408 and 7432, a 5v regulated power supply and logic switch units. Inseart the ICs with the pins 1-7 on one side and pins 8-14 on the other side of the central groove on the bread board. Connect the tve and – ve terminals of the 5v power supply to the two side lines of the bread board which may be called '+5v line' and 'ground line'. Connect the pin 14 of all ICs to this +5v line and pins 7 to ground line.

(ii) Now measure the voltage at the points A, B, C and S for all possible combinations of input voltage at A and B by using a dc voltmeter '0-5v' or a digital multimeter. Record all these voltages in a table.

(iii) Define suitable voltage ranges as 0 and 1 and oftain the truth of the half-adder.

(iv) Construct the full-adder circuit of Fig. 7.5-2 on the bread board as before. Measure voltage at points A_n, B_n, C_{n-1}, S_n and C_n for all possible combinations of the input voltages. Define suitable range as 0 and 1 and verify the truth of the full-adder.

8.6 Experimental Results

IC-7404 (Hex inverter)

IC-7408/7409 (Quad 2-input AND)

IC-7432 (Quad 2-input OR)

(A) Data for input and output voltage for half-adder :

Table I

Input voltage in v at		Output voltage in v at	
A	**B**	**S**	**C**
0.0	0.0	...	...
0.0	5.0	...	...
5.0	0.0	...	...
5.0	5.0	...	...

(B) Truth table as mentioned from Table I :

Define 0.0–0.8v as 0 and 3.0–5.0v as 1

Table II

Input		Output	
A	**B**	**S**	**C**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(C) Data for the input and output voltage for full-adder :

Table III

Input Voltages in V at			Output Voltage in V at	
A	**B**	**C**	$y_1 = S_n$	$y_2 = C_n$
0.0	0.0	0.0	...	...
5.0	0.0	0.0	...	...
0.0	5.0	0.0	...	...
0.0	0.0	5.0	...	...
5.0	5.0	0.0	...	...
0.0	5.0	5.0	...	...
5.0	0.0	5.0	...	...
5.0	5.0	5.0	...	...

(D) Truth table as mertioned from Table III

Define 0.0–0.8v as 0 and 3.0–5.0v as 1.

Table IV

Input			Output	
A_n	B_n	C_{n-1}	S_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

8.7 Discussions

(i) The bread board makes circuit connections highly flexible. There is no need of soldering or using binding screws.

(ii) Unlive analog circuits, here absolute values of the input and output voltages are not important the only requirement is that these voltages must be high or low and lie within certain specified ranges.

(iii) Three LEDs with proper current limiting resistances can be used at the points A, B and Y for easy, quick and visual identification of ‘0’ and ‘1’ states. If a LED glows then it is a ‘1’ state and if it does not glow then it is a ‘0’ state.

(iv) Implementation of digital gates by using IC is more popular than their implementation by using discrete circuit components. This is due to low cost, small size, low power requirement and improved performance of ICs.

(v) While connecting the +5v dc supply to the ICs, care should be taken. Connection to any wrong pin may damage the IC.

(vi) Here the circuits have been designed by using basic gates. The circuits can be conveniently designed by using Ex-OR ICs (7486).

8.8 Summary

With the help of half adder, we can disign circuits that are capable of performing simple addition with the help of logic gates.

Though the implementation of larger logic diagrams is possible with the full adder logic a simpler symbol is mostly used to represent the operation.

8.9 Exercise and Answer

★ **What is clock?**

➢ Clock is usually multivibrator to generate pulse at an exact frequency to synchronize the logic circuits.

★ **What are set and reset inputs?**

➢ In a flip-flop circuit a set input flips the output to the opposite condition from its initial state. A reset input flops the output back to its initial stage.

★ **What is half-adder? Why is it so-called?**

➢ See, theory of Expt. 7.5 A half adder cannot handle the carry coming from the lower order bits. Thus a half-adder is only a step towards the binary addition and to complite the process are require a full-adder. That is why it is called a half-adder.

★ **What is full-adder?**

➢ See, theory of Expt. 7.5.

★ **Construct a half adden using NAND/NOR only.**

➢ See the suggested work at the end of Expt. 7.5.

★ **What is a latch?**

➢ It is another name for a SR flip-flop which can store 1 bit of information. It is called a latch as the information remains locked or latched in the circuit until driggered into alternate state.

★ **What do you mean by set and reset?**

➢ In a flip-flop the state Q = 1 is referred to as the 'set' and the 'set' and the state Q = 0 as 'reset'.

★ **What is the need of a clocked flip-flop?**

➢ Very often it is required to set or reset the flip-flops in synchnnous with a train of pulses known as clock. Thus the need arises of clocked flip-flops?

Unit 9 ❑ To design a Half Subtractor, Full Subtractor, Adder Subtractor using Full Adder IC

Structure

9.1 Objective

To design and verify Half Subtractor and Full Subtractor using Universal logic gates.

9.2 Introduction

Quite similar to the half adder, a half subtractor subtracts two 1-bit binary numbers to give two outputs, difference and borrow. Since it neglects any borrow inputs and essentially performs half the function of a subtractor, it is known as the half subtractor. Let's write the truth table based on this information and general binary subtraction rules.

$0 - 0 = 1$

$0 - 1 = 1$, borrow 1

$1 - 0 = 1$

$1 - 1 = 0$

A full subtractor accounts for the borrow that a half subtractor neglects. Hence it has three inputs and two outputs.

9.3 Theory

Half Subtractor :

Half Subtractor is a combinational circuit which consists of two binary input variables called minued and subtrahend, and two binary output variables called difference and borrow. In the two bit subtraction result, the lower significant bit is called as difference and higher significant bit is called as borrow. The truth table of the subtractor is given below in that the difference becomes logic '1' when both inputs are different each other and it is equal to logic '0' when both inputs are equal. And borrow is equal to logic '1' when minuend is smaller than subtrahend.

Full Subtractor :

Full subtractor is a combinationd circuit which consists of three binary inputs variables called minuend and subtrahend and two binary outputs variables called difference and borrow out. In this subtraction result, the lower significant bit is called as difference and the higher significant bit is called as borrow out. The truth table of the full subtractor descirbes all the eight possible input variations. The full subtractor results the output are equal to logic '0' when all the applied inputs are equal to logic '0' or most significant bit and any one of the least significant bit is equal to logic '1' and the outputs are equal to logic '1' when all the inputs are equal to logic '1' or any of the subtrahend is equal to logic '1'. The difference is equal to 1 when odd numbers of inputs are equal to 1 from the applied three inputs. The borrow out is equal to 1 if any one of the subtrahend or all the applied inputs are equal to logic '1'.

9.4 Apparatus

Component	Specification	Quantity
AND Gate	IC 7408	1
EX-OR	IC 7486	1
OR Gate	IC 7432	1
IC Trainer Kit	—	1
Patch Chord	—	Adequate

9.5 Experimental Produre

(i) Verify the truth table of the given logic Gates.

(ii) Connection to be made as per the circuit diagram.

(iii) All the possible input variations are to be given.

(iv) Observe the output and verify the truth table.

Full Subtractor

K-Map for Difference

A \ BB_{in}	00	01	11	10
0	0	1	0	1
1	1	0	1	0

K-Map for Borrow (Bout) :

A \ BB_{in}	00	01	11	10
0	0	1	1	1
1	0	0	1	0

Sum (S) $= \overline{A}\,\overline{B}B + \overline{A}\,B\overline{B}_{in} + A\overline{B}\,\overline{B}_{in} + ABC_{in}$

$= \left(\overline{A}\,\overline{B} + AB\right)B_{in} + \left(\overline{A}B + A\overline{B}\right)\overline{B}_{in}$

$= \left(\overline{A \oplus B}\right)B_{in} + \left(A \oplus B\right)\overline{B}_{in}$

Sum (S) $= A \oplus B \oplus B_{in}$

Borrow (Bout) $= \overline{A}B + \overline{A}B_{in} + BB_{in}$

$= \overline{A}B + \overline{A}(B + \overline{B})B_{in} + \left(\overline{A} + A\right)BB_{in}$

$= \overline{A}B + \overline{A}BB_{in} + \overline{A}\overline{B}B_{in} + ABB_{in}$

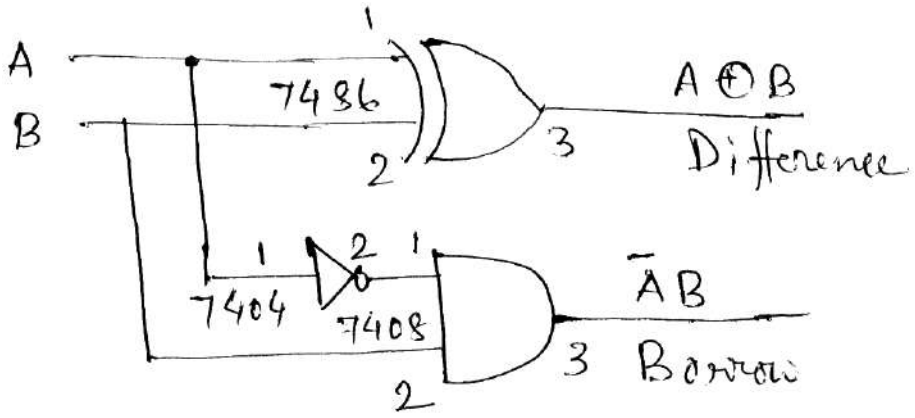
$= \overline{A}B + \overline{A}BB_{in} + \left(\overline{A}\overline{B} + AB\right)B_{in}$

$= \overline{A}B + (A \odot B)\, B_{in}$

(Bout) $= \overline{A}B + \left(\overline{A \oplus B}\right)B_{in}$

9.6 Experimental Procedure

Half Subtractor ⇒



Logic Diagram

Truth Table

A	B	BORROW	DIFFERENCE
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	0

Half Subtractor

K-Map for Difference

A \ B	00	01
00		1
01	1	

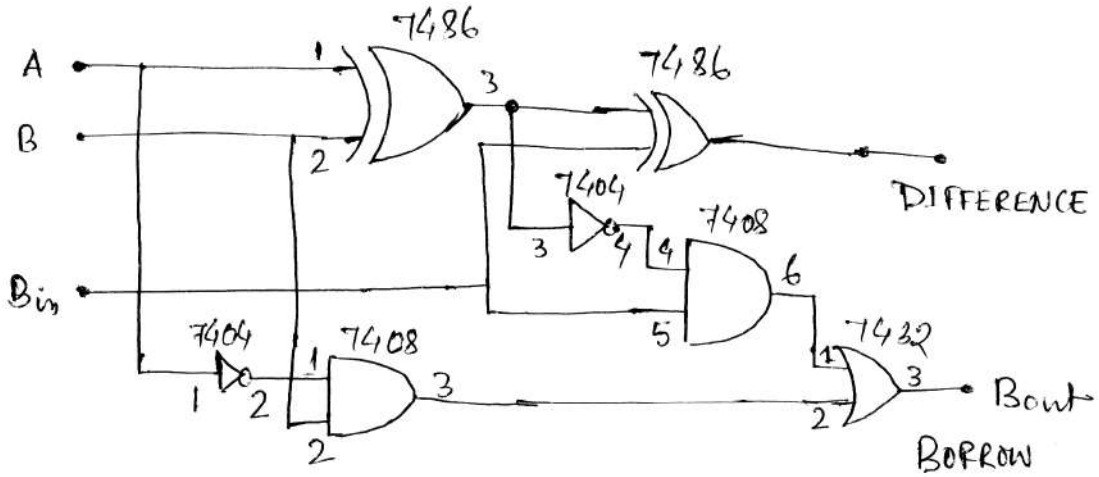
DIFFERENCE = $\bar{A}B + A\bar{B}$

K-Map for Borrow (Bout) :

A \ B	00	01
00		1
01		

BORROW = $\bar{A}B$

Full Subtractor ⇒



Full Subractor using two Half Subtractor.

Truth Table

Input			Output	
A	**B**	**B_{in}**	**B_{out}**	**D**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	1	0	1
1	0	0	0	0
1	1	0	0	0
1	1	1	1	1

9.7 Discussion

You have already learned different binary adder circuits like Half Adder, Full Adder, Parallel Adder and different binary Subtractor, Full Subtractor and also a combination Parallel Adder & Subtractor Circuits.

9.8 Summary

It is possible to convert the full adder circuit into full subtractor by simply complementing the input A before it is applied to the gates to produce the final borrow bit Output (Bout).

9.9 Exercise and Answer

★ **What is clock?**

➢ Clock is usually multivibrator to generate pulse at an exact frequency to synchronize the logic circuits.

★ **What are set and reset inputs?**

➢ In a slip-flop circuit a set input flips the output to the opposite condition from its initial state. A reset input flops the output back to its initial stage.

★ **What is half-adder? Why is it so-called?**

➢ See, theory of Expt. 7.5 A half adder cannot handle the carry coming from the lower order bits. Thus a half-adder is only a step towards the binary addition and to complite the process are require a full-adder. That is why it is called a half-adder.

★ **What is full-adder?**

➢ See, theory of Expt. 7.5.

★ **Construct a half adden using NAND/NOR only.**

➢ See the suggested work at the end of Expt. 7.5.

★ **What is a latch?**

➢ It is another name for a SR flip-flop which can store 1 bit of information. It is called a latch as the information remains locked or latched in the circuit until driggered into alternate state.

★ **What do you mean by set and reset?**

➢ In a flip-flop the state Q = 1 is referred to as the ‘set’ and the ‘set’ and the state Q = 0 as ‘reset’.

★ **What is the need of a clocked flip-flop?**

➢ Very often it is required to set or reset the flip-flops in synohronism with a train of pulses known as clock. Thus the need arises of clocked flip-flops?

Unit 10 ❑ To study the diffraction pattern of a crossed grating with the help of a LASER source

Structure

10.1 Objective

To study the diffraction pattern of a crossed grating with the help of a LASER source.

10.2 Introduction

When n number of slits of same width placed side by side separated by opaque spaces, an optical element is formed produced known as grating. Diffraction pattern produced by a grating is known as grating spectrum. In crossed grating arrangement two gratings are placed at right angles to each other.

10.3 Theory

When an unexpanded laser beam incident normally on the grating the beam of light will be diffracted through the grating and a number of principal maxima of different orders on both sides of central maximum will be formed. If we rotate the grating by 90° from its previous position pattern of the diffracted beam will also rotate by 90°.

When the diffracted order beam produced from first grating is allowed to enter into another grating positioned at right angles to the first one, each diffracted order beam will again be diffracted by second grating and it will produce a diffraction pattern with reticular structure.

10.4 Apparatus Required

Laser source, diffraction grating - two, screen, mount etc.

10.5 Experimental Procedure

(i) Switch ON the laser.

(ii) Place the first grating in the path of laser beam as shown in Fig. 1 and try to observe the diffraction pattern (pattern is shown in Fig. 4). Now rotate the grating by 90°. from its previous position and again try to observe the diffraction pattern (pattern is shown in Fig. 5).

(iii) Place the crossed grating arrangement in the path of laser beam as shown in Fig. 3 and try to observe the diffraction pattern (pattern is shown in Fig. 6).

(iv) Observe the diffraction pattern

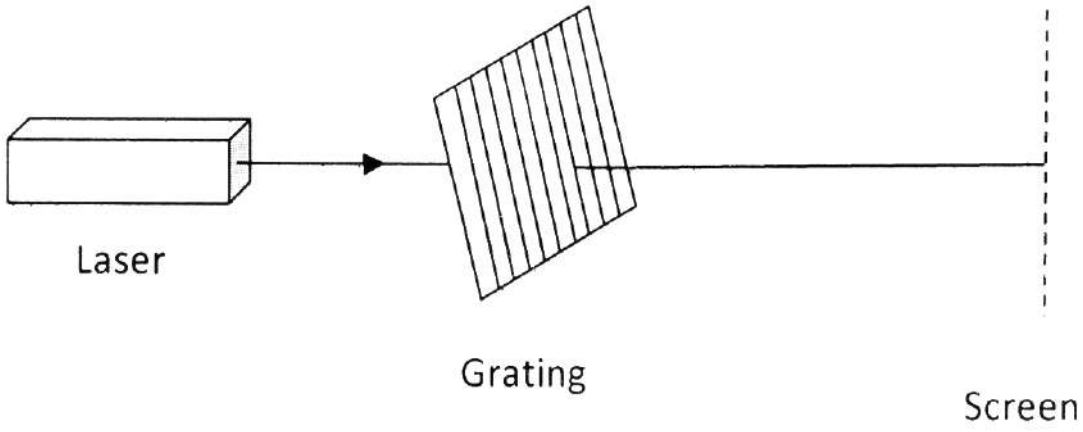


Fig. 1. Experimental setup for observing diffraction pattern from a grating probed by a laser beam.

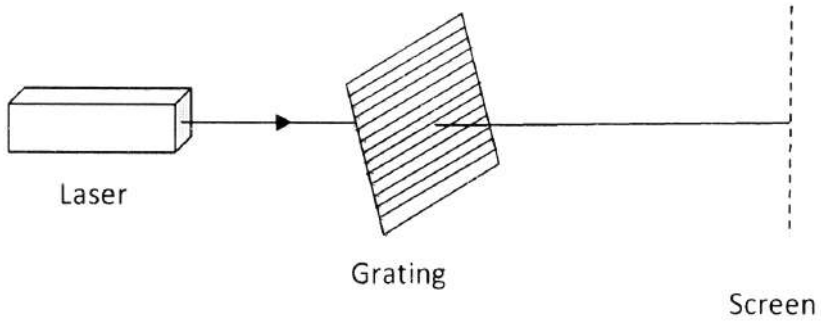


Fig. 2. Experimental setup for observing diffraction pattern from a grating rotated by 90° from its previous position (shown in Fig. l) and probed by a laser beam.

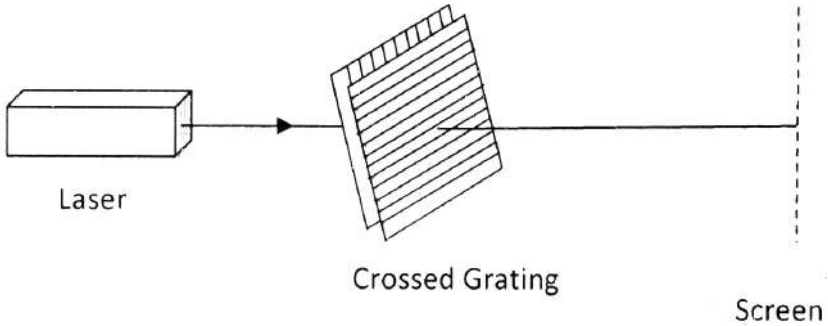


Fig. 3. Experimental setup for observing diffraction pattern from a crossed grating probed by a laser beam.

10.6 Observation

Number of lines per centimetre of I st grating = ... lines/cm
Number of lines per centimetre of 2nd grating = ... lines/cm

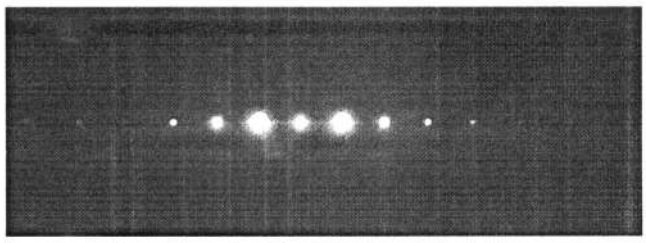


Fig. 4. Diffraction pattern formed by a grating when probed with a laser beam (shown in Fig. l).

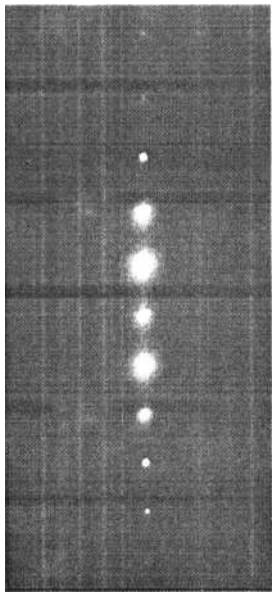


Fig. 5. Diffraction pattern formed by a grating (rotated by 90°) when probed with a laser beam (shown in Fig. 2).

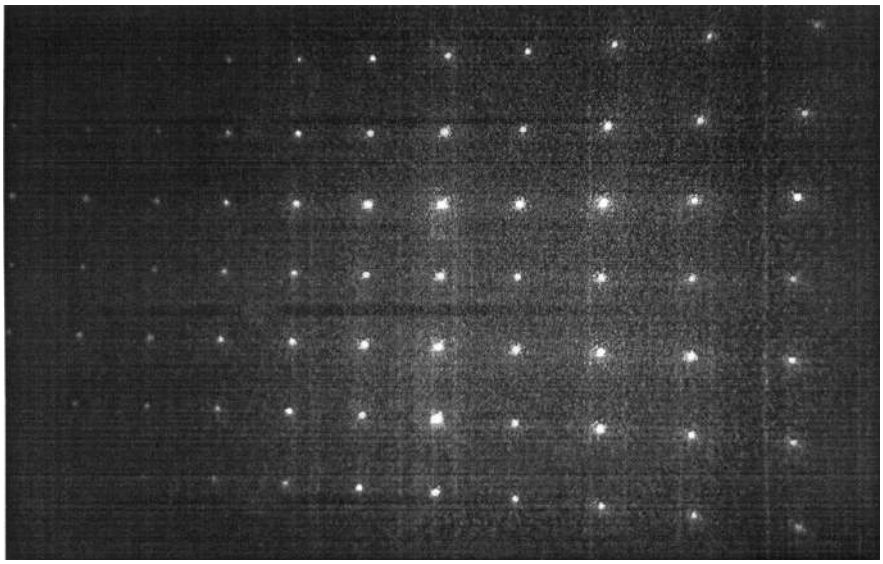


Fig. 6. Diffraction pattern formed by a crossed grating when probed with a laser beam (shown in Fig. 3).

If both the gratings have same grating constant then the pattern will be a square shape otherwise it will be a rectangular shape.

10.7 Precautions

1. Grating surfaces should be normal to the incident rays.
2. Both the gratings should be in crossed position.
3. Never keep your eyes in the path of the laser beam.
4. Do not touch the surface of the grating.

10.8 Oral Questions

1. What is a diffraction grating and how does it work?
2. Define grating constant?
3. What are the uses of diffraction grating?

Unit 11 ❑ To draw the characteristics of a JFET and hence to determine relevant parameters

Structure

11.1 Objective

To draw the characteristics of a JFET and hence to determine relevant parameters.

11.2 Introduction

The difference between bipolar junction transistor (BJT) and filed effect transistor (FET) is : BJT is a current controlled device whereas FET is a voltage controlled device. In case of BJT, input current controls the output characteristics whereas for FET input voltage controls the output characteristics.

Current conduction in FET takes place either by electrons or holes, hence is known as a unipolar device.

Schematic diagram of n-channel JFET and p-channel JFET is shown in Fig. l(a-b)

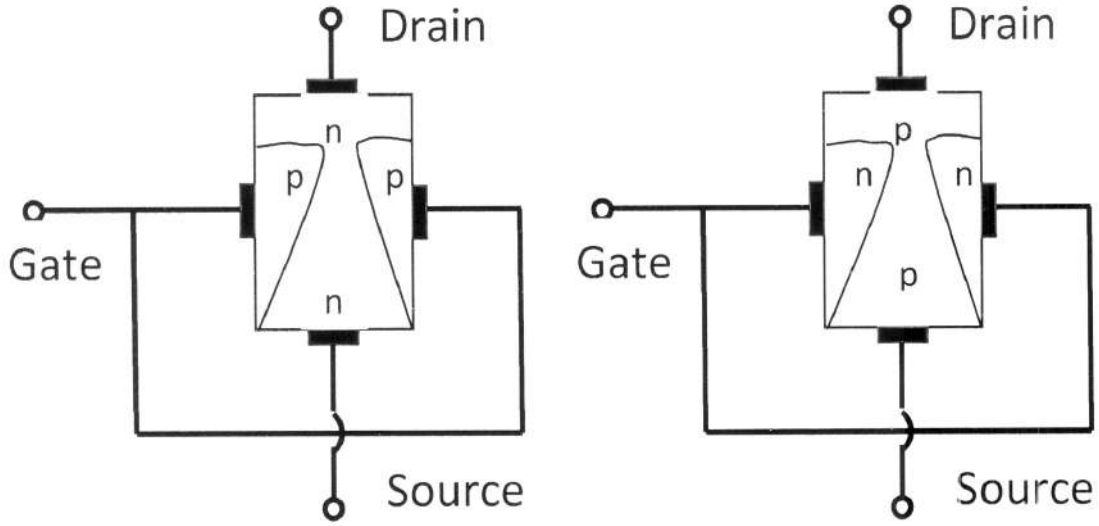


Fig.1. Basic structure of (a) n-channel JFET (b) p-channel JFET.

11.3 Apparatus Required

FET, bread board, resistor, connecting wires, D.C. power supply, two voltmeters, a milli-ammeter.

JFET parameters

(i) **Drain resistance**

$$r_D = \frac{\text{change in drain source voltage}}{\text{change in drain current}} \text{ at constant } V_{GS}$$

(ii) **Transconductance**

$$g_{fs} = \frac{\text{change in drain current}}{\text{change in gate-source voltage}} \text{ at constant } V_{DS}$$

(iii) **Amplification factor**

$$\mu = \frac{\text{change in drain source voltage}}{\text{change in gate-source voltage}} \text{ at constant } I_D$$

Relationship among JFET parameters

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}; \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \times \frac{\Delta I_D}{\Delta I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}; \quad \mu = r_d \times g_{fs}$$

11.4 Experimental Procedure

Output Characteristics

(i) At first connect the circuit as shown in Fig. 2.

(ii) Keep V_{GS} = 0V and vary Drain-Source voltage V_{DS} in step of 0.5 volt and note the values of Drain-Source voltage V_{DS} and corresponding values of Drain current I_D till the Drain current becomes constant.

(iii) Keep the Gate-Source bias at – (...)V and note the values of Drain-Source voltage V_{DS} and corresponding values of Drain current I_D till constant readings of I_D are obtained.

(iv) Repeat with a Gate- Source bias of – (...)V.

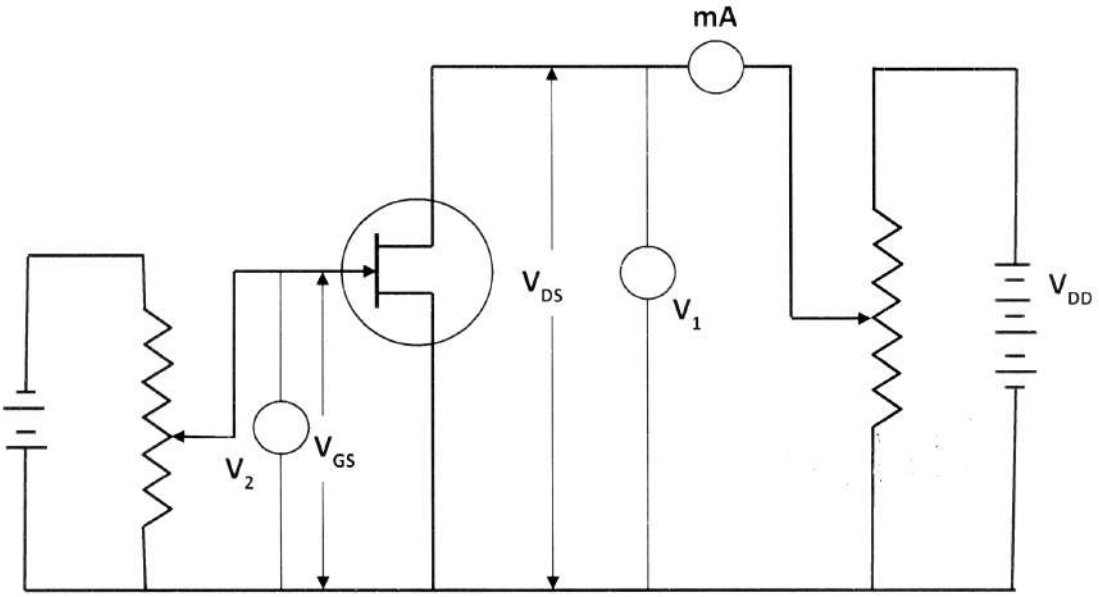


Fig 2. Circuit for determining characteristics of JFET.

Transfer Characteristics

(i) Set the Drain-Source voltage V_{DS} constant at + (...)V (as per the data of FET used)

(ii) Vary the Gate-Source voltage V_{GS} from zero towards negative values in steps of 0.5V.

Note the values of V_{GS} and corresponding values of Drain current I_D. As the negative Gate Source voltage increases the Drain current I_D decreases, take the reading till the current I_D becomes zero.

(iii) Similarly repeat with Drain Source voltage of + (...)V.

Observation

TABLE 1. Output characteristics

Sl. No.	V_{GS} = 0V		V_{GS} = – (...)V		V_{GS} = – (...)V	
	V_{DS}	I_D	V_{DS}	I_D	V_{DS}	I_D

TABLE 2. Transfer characteristics

Sl. No.	V_{DS} = (...)V		V_{DS} = (...)V	
	V_{GS}	I_D	V_{GS}	I_D

Graph

(i) For output characteristics, plot graphs between Drain current I_D (along Y-axis) and Drain-Source voltage V_{DS} (along X-axis) for various values of Gate-Source voltage V_{GS}.

(ii) For transfer characteristics, plot graphs between Drain current I_D (along Y-axis) and Gate Source bias V_{GS} (along X-axis) for various values of Drain Source voltage Y_{DS}.

Calculation

(i) from drain characteristics Drain resistance can be calculated.

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

(ii) from transfer characteristics Transconductance can be calculated.

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

(iii) Amplification factor can be calculated by Drain resistance and Transconductance value.

$$\mu = r_d \times g_{fs}$$

Result

1. r_D = ...
2. g_{fs} = ...
3. μ = ...

11.5 Precautions

1. Check maximum rating of FET up to which it can be used.
2. According to n-channel or p-channel FET apply the Gate-Source voltage and Drain Source voltage.
3. Connections should be tight.

11.6 Oral Questions

1. What is the difference between BJT and FET?
2. What is Transconductance?
3. What is pinch off voltage?
4. What is Shorted gate drain current?
5. What is Gate to source cut off voltage?

Unit 12 ❑ Determination of thickness of a thin film by using Fresnel's bi-prism

Structure

12.1 Objective

To determine the thickness of a thin sheet of mica with the help of Fresnel's biprism

12.2 Introduction

The Results of Young's double slit experiment quite clearly indicate interference and the wave nature of light, when the experiment was first done objections were raised that the results were not conclusive since there could have been difference effect from the edge of the slits. To counter this, Augustin Fresnel proposed a series of interference experiments that would have no diffracting edge. The most notable of these is the Fresnel's Biprism, where two virtual source are created by refraction through a biprism.

12.3 Theory

It, in Fig. 12.3-(i), a thin sheet of mica of thickness t is introduced in the path of one of the interfering beams by covering one-helf of the biprism with mica sheet, the optical path length of the beam increases by $\frac{t(\mu-1)}{\lambda}$ when μ is the refractive index of the sheet for the wave length λ of the light used. As a result, the frige patttern on the serean AB is displaced towards the beam in the path of which the mica sheet is placed. If s is the shift of the central fringe on the screen and x is the fringe width, the increase in the optical path is also given by s/x wave lengths. So,

$$\frac{t(\mu-1)}{\lambda}=\frac{s}{x} \qquad \text{..... (i)}$$

But $$\lambda=\frac{xd}{D} \qquad \text{..... (ii)}$$

where d is the distance between the virtual sources S_1 and S_2 and D is the distance between the slit and the screen.

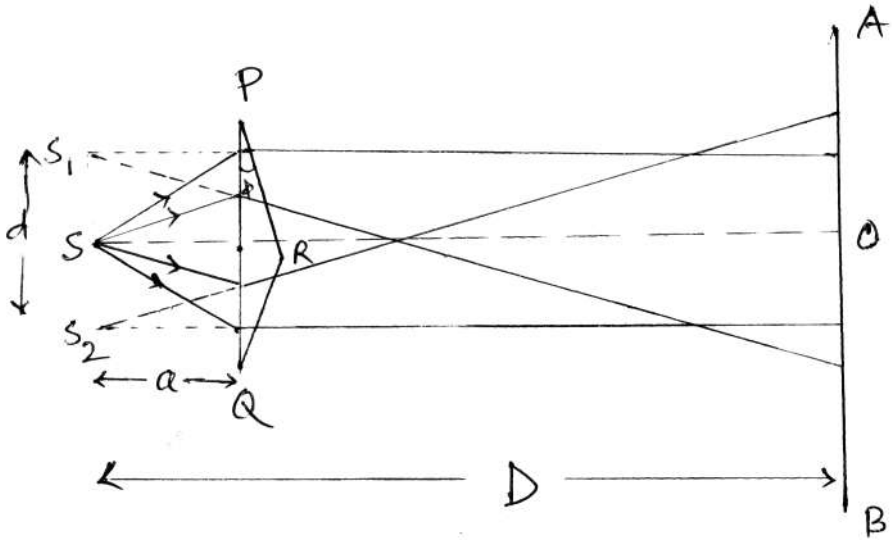


Fig. 12(i)

Noting that $D = D_1 + \beta$, where D_1 is the aparent distance between the slit and the focal plane of the eye-piece, and β is the index error, we obtain from (i) and (ii)

$$t = \frac{sd}{(D_1 + \beta)(\mu - 1)} \quad \text{..... (iii)}$$

The index correction can be avoided by observing the shifts s_1 and s_2 for two apparent distance D_1 and D_2 between the slit and focal plane of the eye-piece respectively.

Then eq. (iii) gives

$$D_1 + \beta = \frac{s_1 d}{t(\mu - 1)} \quad \& \qquad D_2 + \beta = \frac{s_2 d}{t(\mu - 1)}$$

$$\therefore\ D_2 - D_1 = \frac{d(s_2 - s_1)}{t(\mu - 1)}$$

or, $$t = \frac{d}{\mu - 1} = \frac{s_2 - s_1}{D_2 - D_1} \quad \text{..... (iv)}$$

To determine d, a convex lens whose focal length f is such that D is greater than if, is placed between the biprism and the eye piece. For two positions of the lens, real images of the virtual sources s_1 & s_2 are obtained on the focal plane of the eye-piece. If d_1 and d_2 are the distance between the real images of s_1 and s_2 for the two positions of the lens, then

$$d = \sqrt{d_1 d_2} \quad \text{..... (v)}$$

12.4 Apparatus

(i) A Feresnel biprism

(ii) an source of menochromatic light

(iii) a source of white high

(iv) a slit

(v) micrometer eye-piece

(vi) a convex lens of suitable focal length

(vii) an optical bench with four stands

(viii) a plump line

(ix) an index rod (if required)

(x) a thin mica sheet and

(xi) a clamped stand (if required)

12.5 Experimental Procedure

The procedure consists of two parts : (a) adjustment, and (b) measurements

(a) Adjustments :

1. Mount the upright carrying the slit near the zero on the scale on the optical bench. Set up a phemp line near the slit and make the datter vertical by the tangent screw attached to it. Look along the axis of the bench from the other end and bring the slit in the middle of the bench by moving the slit stand perpendicular to the bend. Make the slit very narrow by the screw for adjusting the slit width.
2. Mount the biprism on its stand with its plane face dioected towards the slit and at right angles to the optical bench. Move the stand towards the slit until it is in contact with the slitstand. Adjust the height of the biprism on that the centre of the biprism and that of the slit are in the same height.
3. Illeminate the slit and sodium light and adjust the position of the flame so that its brightest part of in the front of the slit. Place a screen with a linear apperture between the slit and the source to cut off any stray light. On looking at the slit through the biprism along the middle line of the optical path, turn the transverse screw of the biprism till the common base of the biprism is found to move across the slit. Then places the biprism in the middle of the bench. If there is an appreciable angle between the slit and the base of the biprism, adjust the tangent screw of the biprism till they are parallel.
4. Place the upright carrying the eye piece on the optical bench and close to the biprism. Adjust the height of the eye piece so that its axis may be at the same height at the centre of teh biprism. Focus the eye piece on the cross

wires and move it perpendicular to the length of the bench until its axes passes through the centres of the biprism and the slit. Now intistinct fringes appear in the field of view.

If on looking through the eye piece you nither find a fringe system nor a bright patch of light in the field view, turn the transverse screw of piprism till it is found. Then make fringes as distinct as possible by rotating the prism in own plane by tangent screw.

5. After getting well defind fringes when the bases of slit stand and the biprism stand are in contact proceed to cheeck whether d_1 and d_2 will be observable. For this, take canvex lens for d_1 and make a rough estimate for focal length. Shift eyepiece slowly and place it at 4.5 times the focal length from the slit. While moving eye piece, take care that the fringes never go out of sight. To keep the fringes in the field view, adjust the transverse screw of biprism continuously.

   Now mount the lens on the optical bench with an upright between prism and eyepiece. Adjust height and position so that centre is an the line joining everything move the lens along bench to get real image of virtual source s_1 and s_2 in the focal plane of the eye piece for two position of the lens.

6. Remove the lens from the bench. Slowly shift the upright carrying eyepiece away from biprism and place it near the end of optical bench. While moving eyepiece keep fringes in field view by adjusting transverse screw. If intensity decreases with distance, adjust slit width, position and intensity of sodium flame. If fringes are too broad, move the biprism slowly away from slit till fringe width lie within 1 to 2 milimiters. Note that the biprism must not be moved to a distance greater than that corresponding to the position of the lens nearer to the biprism in the previous operation.

7. Place and switch on a high power electric lamp behind the sodium flame. Adjust in height so that the incandescent filament is at the same height as the axis of the eye piece. Coloured fringes with a white one at centre will be observed in field view. Bring the central fringe on the cross wires by adjusting transverse screw of eye piece. Move the eye piece close to prism,

keeping central fringe on the cross wire by adjusting micrometer screw. Next move eyepiece away from biprism and bring it near end of optical bench. Keep the central fringe on the cross wires by continuously adjusting the transverse screw. This are repeated till the central fringe is an the cross wires for all position of eye piece.

(b) Measurments :

1. Remove the white light. Determine the vernier constant for bench stands and the least count for the micrometer of eye piece. Fix the eye piece at a distance of about 4.5 times the focal length from the slit. Place the stand carrying the lens of the optical bench between biprion and eye piece, make it coanial with the latter. Now on moving the lens stand along the bench, magnified real image of virtual sources s_1 and s_2 will be seen in the field of eye piece. Bring the images at equal distances from the cross wires by rotating lens about vertical axis. This ensures that images of both s_1 and s_2 appear simultaneously in focus at each of the two positions of the lens. Measure the distance d_1 between two frings by shifting the eye price perpendicular to the bench and setting the cross wires on the same eye (left or right) of the image. Make this measurement four times, once shifting the eye piece frame left to right again fram right to left. The mean of four values gives d_1. Re-adjust the lens in this position repeat readings for the more independent settings of lens. Take mean value for d_1.

   Next move the lens towards the eyepiece keeping the latter fixed in previous position till sharp images of virtual sources s_1 and s_2 are seen in field view. Determine the distance between of two images d_2 in a same manner. From this value of d_1 and d_2, d is calculated from Eq. (vi) [If time permit determine d for two other position of eyepiece on bench, close to previous position. Use mean value to calculate t. Note that in each case the position of eye piece should be such that its distance from slit is greather than 4 times the focal length of lens'.

2. Replace the sodium light by an incandescent lamp (white light) so that a central white fringe flanked by a few coloured fringe is obtained. So the

cross wires of the eye piece on the white fringe and take the reading of the micrometer screw.

The stand carrying the mica sheet is now so placed that the mica sheet covers only one half of the prism. Using a lateral motion screw and looking towards the slit and start edge of the mica film is made parallel to the prism edge. This answers that the sheet is introduced in the path of only one of the intefering beams. The fringe pattern is displaced consequently. Shift the eye piece by furning the micrometer screw and set the cross wires of the eye piece on the white frings again. Take the reading of the screw. The difference between the two readings given the shifts of the pattern on the insertion of the mica sheet. Measures once again by removing the mica sheet and shifting the eye piece in the reverse direction. Take the mean of these two values. Repeat the readings for two more impedent settings of the mica sheet. Find the grand means.

3. Read D_1.
4. If the index correction is to be avoided, repeat the step 2 for another distance D_2 of the eye piece without changing the positions of the slit and the Biprism.
5. If the index correction is required find the error β as in Exp. No. 01. Taking value of μ for mica for the D-line of sodium from Physical tables, Calculate the thickness t from Eq. (iii) and Eq. (iv).

12.6 Experimental Results

Table 1

Measurement of the slights of the fringe pattern.

(a) Position of the slit on the bench = ——— + ——— = ——— cm

(a) Position of the biprism on the bench = ——— + ——— = ——— cm

(a) Position of eye piece on the bench = ——— + ——— = ——— cm

Apparent distance between the slit and the eye piece.

$D_1 = (c - a)$ cm

No. of obs	Position of mica sheet on the bench	Direction of eye piece move-ment	Reading (mm) of the micrometer screw for the eye piece set at the central white fringe						Pattern shift ($x_2 \sim x_1$) (mm)	Means (cm)	Grand mean (cm)
			without the mica sheet			with mica sheet					
			Linear	Circular	Total (x_1)	Linear	Circular	Total (x_2)			
1.	.....	forward	.....	.....	.....	.....	.....	.....	.....	.....	
		backward	.....	.....	.....	.....	.....	.....	.....		
2.	.....	forward	.....	.....	.....	.....	.....	.....	.....	.....	.....
		backward	.....	.....	.....	.....	.....	.....	.....		
3.	.....	forward	.....	.....	.....	.....	.....	.....	.....	.....	
		backward	.....	.....	.....	.....	.....	.....	.....		

Table 2

Today error between the slit and the eye piece

Position of the slit a_1 (cm)	Position of the eyepiece when the end of the rod is in clear focus a_2 (cm)	Apparent length of the rod $l_1 = (a_1 \sim a_2)$ cm	Actual length of the rod l_2 cm	Index error $\beta = (l_1 - l_2)$ cm
.....	.....	.....	.....	.....

Table 3

Determinatia of teh thickness of the mica sheet (meaning the index correction)

Distance (cm)	Apparent distance D_1 (cm)	Index error β (cm)	$D_1 + \beta$ (cm)	Pattern shift (cm)	Frefractive index of mica μ	Thickness t (cm)

[The table for determining t avoiding the index correction is left for the Hudeep to male]

12.7 Discussion

1. In the measurement of the distance (d) between the two virtual sources S_1 and S_2, the distance between the slit and the screen should be nearly equal to 4.5 times the focal length of the Convex Lens so that d_1 and d_2 do not differ largely. This will reduce the error is measuring d.
2. While using the micrometer screw, core should be taken to avoid back lash error arising from the misfit between the micrometer screw and the nut in an old instrument. To do this, the eye-piece should be moved beyond the image cocerned before reversing its direction of movement from left to right, or vice versa. One can also find the distance from the initial and final readings of the screw and counting the number of complete turns without depending on the linear scale.
3. While measuring d_1 and d_2. the images may be distored due to spherical aberration. To avoid this distortion, a stop with a passage of light through the central portion of the lens may be used.

N.B. : If possible, repeat the experiment for another value of D_2, say D_3. Calculate three a values of λ from Eq. (v) for $D_2 \sim D_1$, $D_3 \sim D_2$ and $D_3 \sim D_1$, and find mean λ. If, however, any of the three differences, $D_2 \sim D_1$, $D_3 \sim D_2$ and $D_3 \sim D_1$ is quite small, the percentage error in λ will be large. In that case calculate three values of λ from Eq. (iv) for D_1, D_2 and D_3 making index correction and obtain the mean 'λ'.

12.8 Summary

Fresnel's biprism can be used to determine the wavelength of a light source (monochromatic light), refractive index of medium etc. Fresnel's biprism retracts and produces two virtual images which acts like cohorent sources. An interference pattern is produced which can be seen with an eye piece.

12.9 Exercise and Answer

1. In the Fresnel biprism experiment, how are two coherent sources realisted?

Ans. The two virtual sources produced by refraction of light from a single source through the two halves of the biprism, serve as the two coherent sources in the Fresnel biprism experiment.

2. If, instead of a monochromatic light white light is used in Fresnel biprism experiment, what will you see in the fringe system?

Ans. While light is a combination of seven colours the path difference between two interfering rays is zero for all wavelengths. Hence the central fringe will be while. Again the spacing between two consecutive bright or dark fringes decreases with the decrease of wavelength [Eq. (i)]. As a result, the bright fringe nearer to the central fringe will have strong violet tinge, followed by other bright fringes having a strong fringe of colours in the spectral order. After some fringes the path difference between two interfering light waves becomes so large that the conditions for constructive and destructive inference may be satisfied at a given point simultaneously for a number of wavelengths. So, the dark fringes of some wavelengths are completely marked by the bright fringes of other wavelengths. Moreover, at some points, so many colours may superpose that the resultant illumination essentially appears white.

3. Who do you use a narrow slit? What will be the effect on the fringes if you broaden the slit?

Ans. A narrow slit is used because it produces distinct fringes.

When the slit is gradually broadened, the fringe system first becomes blurred, because a broad source will serve as many narrow sources will produce two coherent virtual sources and the fringe system due to one pair of virtual sources will not be formed exactly in the same position as that due to other pairs, resulting in a blurred fringe system.

When the slit is sufficiently broadened, the dark fringes due to one pair of virtual source will be completely marked by the bright fringes due to another pair. As a result no fringe system will be observed.

4. What is the order of angle of the biprism, ϕ? What will happen if ϕ is increased?

Ans. About 30'. When ϕ is increased, d increased and the fringes become narrower.

5. What will happen if one half of the bipirism is covered with lamp block?

Ans. The fringes will disappear because one of the two coherent sources will be removed.

6. Can the covex lens in the experiment have any focal length?

Ans. No. the focal length f should be such that D > 4f. Only then the real images of the virtual sources can be focused at the focal plane of the eye piece.

7. Why do you take a thin mica sheet?

Ans. Because, if the mica sheet is thick the fringe pattern will be displaced significantly. The central fringe may then go beyond the range of movement of the micrometer screw of the eye-piece.

8. Will the fringe width change open the insertion of the mica sheet?

Ans. No.

9. If the mica sheet is introduced in the path of both the interfering beams, what will happen?

Ans. There will be no shift of the fringe pattern, because the optical paths of the two interfering beams change equally.

10. What is 'optical path'?

Ans. It is the product of the geometrical path length traversed by light and the refractive index of the medium.

11. Why do you use white light to measure 's'?

Ans. With white light, the central fringe is white, and so it can be readily located. This facilitates the measurement of S. If a monochromatic source is used, the shift of the central fringe can not be measured because all the fringes 100 K identical.

12. Can you measure the refractive index of mica in your experiment?

Ans. Yes; if the thickness t of the mica sheet is known, its refractive index μ can be found from Eq. (iii), the other quantities being measured in this experiment.

13. Why do you choose mica here?

Ans. Because mica sheets can be made very thin.

Unit 13 ❑ To Calibrate a thermocouple to measuere temperature in a Specified Range using (i) Null Method (ii) Direct measurement using Op-Amp difference amplifier and to determine Neutral temperature

(i) Null Method

Structure

13.1(i) Objective

To draw the thermo emf-temperature curve of a given thermocouple and to caliprate the thermocouple to measure temperature in a specified range.

13.2(i) Introduction

Ordinarily a copper-constantan couple is employed for this experiment. The couple gives about 40 micro-volt per 0°C. To prepare this couple, three pieces of wires, each of one meter long are taken, of which one is of constantan while the other two are of copper. The two ends of constantan wire are cleaned and are joined by twisting with one end of each of the copper wires. The junctions are then soldered with minimum amount of solder covering a length of about 2 or 3 mm of each

junction. Two glass are introduced in the copper wires to be sure that the metals touch at the junction only.

13.3(i) Theory

When one junction of a thermo-couple is kept at 0°C while its other junction is maintained at a higher temperature, thermo-emf e will be developed in the couple. If this emf e be balance against the potential difference existing at the ends of a length of potentiometer wire of total length L having the potential drop P per Unit length then.

$$e = Pl$$

If E be the emf of the storage bettery B, R be the resistance of the potentiometer wire of length L and R_1 be the resistance applied in the resistance box kept in the potentiometer circuit then

$$P = \frac{ER}{(R + R_1)L}$$

From we get

$$e = \frac{ERl}{(R + R_1)L}$$

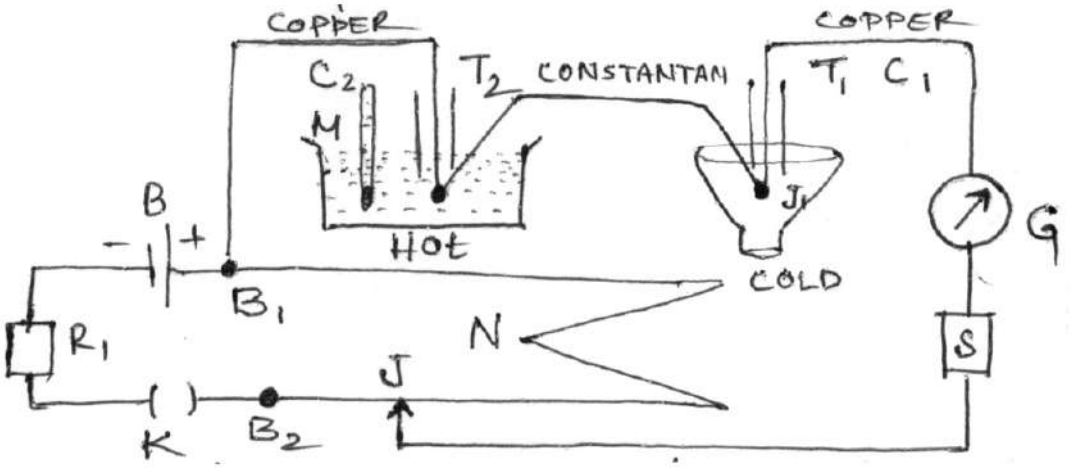
By measuring thermo-e.m.f. e with the help of Eq. for different temperatures of the hot junction, a curve may be drawn by plotting temperature (t°C) of the hot junction along the x-axis, while the corresponding thermo-emf e along y-axis. Within a small range of temperature (which is far away from neutral temp) the curve would be a straight line as is shown in Fig. This curve is called the calibration curve of the given thermo couple.

To find the thermo-electric power $P = \frac{de}{dt}$ at a given temperature 0°C of the hot junction a tangent is drawn to curve at the point corresponding to θ°C of the hot junction. By measuring to slope (BC/AC in Fig.) of this tangent line $P = \frac{de}{dt}$ can be determined at θ°C. If e is measured in μV and t in °C then P will be given in units of μV/°C.

To find the unknown temperature one junction of the thermo-couple is kept at 0°C while its other junction is kept within a bath of unknown temp (7°C). Then by measuring the thermo-emf e from the relation the unknown temperature can be found out from the calibration curve (as the temperature corresponding to the emf e).

13.4(i) Apparatus

(a) A potentiometer (b) a Galvanometer (c) a Battery (usually Alkali cell) (d) a Plug key (e) two Resistance box (f) Copper and Constant wire (g) a tunnel (h) two thermometers (i) Crushed ice.

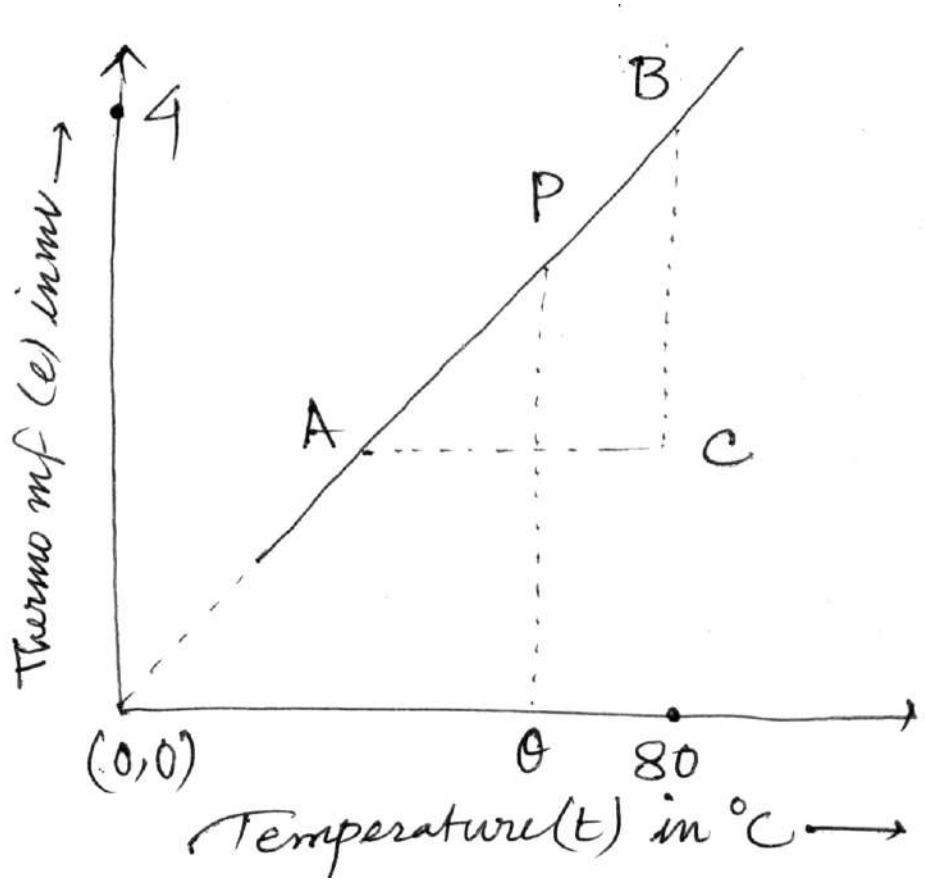


13.5(i) Experimental Procedure

(i) The resistance R of the potentiometer wire is measured by a P.O. box. the emf E of the storage battery B is measured by an occurate voltmeter reading 0.0/volts. The emf of the battery B, should be measured also after the experiment to see whether if remained constant throughout the experiment or not.

(ii) A thermo couple is constructed from the supplied wires as described earlier.

(iii) To make the process of null point (l) determination easier and time saving and at the same time kuping the order of accuracy same as in the measurment of the quantities, it is usual to choose a proper value of R_1 and to keep it constant throughout the experiment.



If we take the usual copper constantan couple & draw the calibration curve for a maximum temperature difference of 100°C then a p.d. of 5 μV/cm along the potentiometer wire will give a null point at the middle of the 10th wire with the hot junction at 100°C.

The required value of R_1 is calculated from the relation by putting $P = 5 \times 10^{-6}$ V/cm. The applied value of R_1 is a hound number near about the calculated value of R_1.

(iv) After making connections of circuit in the manner as shown in Fig, the hot junction J_2 is introduced into water at room temperature (t_1°C). [If $t_1 \sim 30$°C, the null point may vbe obtained near about the 3rd wire]. After finding a rough null point with a high resistance S, the value of S should be made zero to get the accurate null point. This null point is noted several times and their mean value (l_1) is obtained.

From this mean value of null point, the thermo-emf (e_1) at room temperature (t_1°C) is calculated by the relation.

(v) Temperature of water (in which the junction J_2 is kept immersed) is now raised by steps of 10°C and at each setp, several rull points are noted by constantly stirring the water and maintaining its temperatrue constant for at least 3 or 4 minutes. The mean value of several null points at each temperature by using the relation proceding in this way, the final mean null point is determined at a temperature (t_2°C) of about 90°C and the corresponding thermo-e.m.f. is also calculated from the relation.

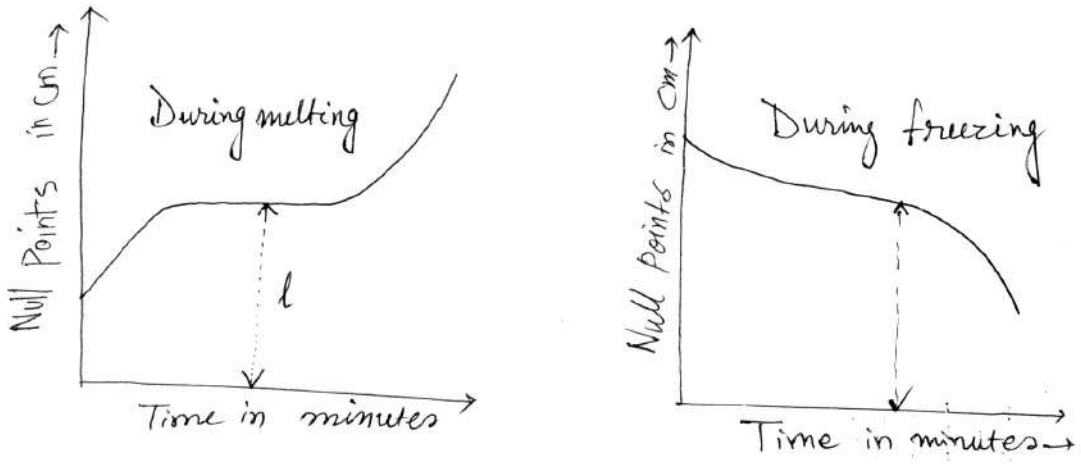
(vi) A graph is then drawn by plotting the temperature (t°C) of the hot junction along x-axis and its corresponding thermo-emf e (in mV) along y-axis. This curve is called the calibration curve of the thermo-couple. As the neutral temperatrue of the couple is far away from the highest temperature employed for the hot junction and as the range of temperature employed is small, the curve would be a straight line as in shown in the Fig.

(vii) To find the thermo-electric power $P\left(=\frac{de}{dt}\right)$ at a given temperatrue θ°C a tangent is drawn to the calibration curve at a point corresponding to θ°C. Form the stop of this tangent we get $P=\frac{de}{dt}=\frac{BC}{AC}$ in mV/°C.

(viii) The hot function J_2 is now immersed in an unknown temperature bath. Generally as an unknown temperature the students are asked find the melting point of a solid. The powdered solid (whose milting point is required) is taken in sufficient amount in a test tube the hot junction J_2 of the couple is introduced at the middle region of this powder. The test tube is then introduced in the water taken in a large beaker. The temperature of this water can be varied. The resistance R_1 is kept unaltered in the potentiometer circuit and the null points on the potentiometer wire are noted after an interval of half minute from the beginning of multing of solid till the whole of half minute is adopted from the beginning of feeling of liquid till the

whole of it melts. The same procedure of noting the null points, after an interval of half minute after an interval of half minute is adopted from the beginning of freezing of liquid till the whole of it is solidified.

(ix) Two curves are drawn by plotting time along x-axis and corresponding null points along y-axis. The nature of the curves will be like those shown in Fig. (during the melting of solid] and in other fig. [during the fruzing of liquid]. Both the curves will blow a horizontal part when the melting or freezing in going on. The ordinate *l*' of this horizontal part will be the actual null point. The mean of these two values of *l*' (one during multing and another during fruzing) in employed to calculate thermo-emf *l*' corresponding to the melting point T°C of solid, by using the Eg.



(x) The melting point of the solid is now found out the calibration curve as the temperature corresponding to the thermo-e.m.f. *l*'.

13.6(i) Experimental Result

(A) Determination of the resistance (R) of Pot. wire :

Table I

Value of Q (1st arm) in Ω	Value of P (2nd arm) in Ω	Ratio Q/P	Resistance in the third arm in Ω(R)	Galvanometer deflection	Nature of resistance in the R-arm, in comparison with the unknown resistance (x)	Unknown resistance (X) in Ω
10	10	1	5000	right	too high	X lies between 60 & 61Ω
			0	left	too low	
			100	right	too high	
			50	left	too low	
			60	slightly left	slightly low	
			61	slightly right	slightly high	
10	100	$\frac{1}{10}$	607	right	high	X lies between 60.5 & 60.6Ω
			606	slightly right	slightly high	
			605	slightly left	slightly small	
10	1000	$\frac{1}{100}$	6055	slightly left	slightly small	X = 60.56 Ω
			6056	no deflection	equal	
			6057	slightly right	slightly high	

(B) Nothing of the EMF(E) of the cell B

Table II

Stage of Expt	EMF of cell B in V	Mean EMF in V	Remark
Before Expt	.....	.....	The emt of battery is remaining constant
After Expt	.....		

(C) Calculation of R_1 :

From Eq. $R_1 = \frac{ER}{PL} - R$

Putting P = 5×10^{-6} V/cm (for Cu constantant couple)

L = 1000 cm and the measured values of E & R we can calculate R_1

(D) Temperature – Null point record :

Temp. of cold junction = 0°C

EMF of battery B = E = ... V

Res of Pot wire = R = ... Ω

Length of Pot. wire = L = 1000 cm.

Table III

No of Obs	Temperature of hot Junction in °C (t)	Resistance in the pot circuit in Ω (R_1)	Null Points			Total length in cm required for balance (l)	Thermo emf $l = \frac{EMl \times 10^3}{(R+R_1)L}$ in mV
			On wire no.	At the scale readings in cm	Mean scale readings in cm		
1.	Room temp = t_1°C	.....	3rd	19.9 19.8 19.7 51.9	19.8	219.8	.....
2.	t_1 + 10	.....	4th	51.8 51.7	51.8	348.2	.....
etc	etc	etc	etc	etc	etc	etc	.....
3	.....	.....	.....	....	.....	.....	.....

(E) Drawing of (e – t) curve, the temperature (t) of the hot junction in °C is plotted along x-axis while the corresponding thermo-emf (e) in milli volts is plotted abiog y-axis. As the range of temperature is small and the highest temperatrue applied at the hot junction far below the neutral temperature, the curve would be a straight line (straight portion of a parabola). The nature of the curve is shown in the fig.

(F) To find thermo-electric power from the graph at a specified temperature

Table IV

Temp θ in °C	Δe = Bc in mV	Δe in μV	Δt = Ac in °C	Value of $\frac{\Delta e}{\Delta t}$ in μV/°C
.....	.....	.....	.....	.....

(G) Time-Null point record during melting & freezing of the solid : Temperature of fold Junction = 0°C, Resistance R_1 = ...Ω

Table V

	Null point during melting			Null point during freezing		
Time in min	wire no.	Scale read in cm	Total length in cm	Wire no.	Scale read in cm	Total length in cm
0						
$\frac{1}{2}$						
1						
$1\frac{1}{2}$						

ii) The water taken in the beaker (in which hot junction J_2 is introduced) should be large and it should be heated slowly so that the temperature may remain constant for an appreciable time.

iii) The function (J_1 and J_2) should be kept at the middle region of the bath so that the temperatures of the functions may not change due to a small variation of the temperature of the surroundings.

iv) The experiment should be performed within a small range of temperature so that the (e – t) curve writhin that range may be approximately a straight line.

(ii) Direct measurement using Op-Amp

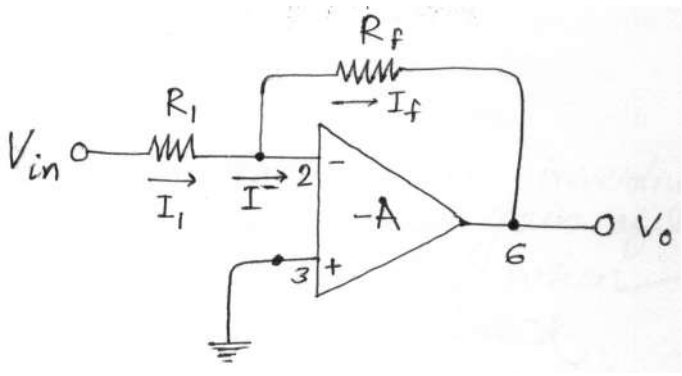
Structure

13.1(ii) Objective

To draw the thermo emf-temperature of a given thermo-couple and to calibrate the thermocouple to measure in a specified rangs.

13.2(ii) Introduction

Let us now consider the most commonly used op-amp circuit. This circuit will be used in measuring thermo emf. It is called inverting amplifier. It is so called because the non-inverting input is grounded and the input voltage V_{in} is comucted through resistor R_i to the inverting input. The resistance R_t is called the feedback resistor, because it feeds part of the output back to the input. If voltage at the input end is V_i and the output voltage is V_0. We have $V_0 = - AV_i$.



Now voltage gain is –A, negative because the amplifier is in an inverting mode. We notic $V_{in} \neq V_i$, there is a resistance between them. A is OP amps inhert gain when there is no feed-back loop, it is often called open-loop gain of the OP-amp.

From Ohm's law we can write

$$I_1 = \frac{V_{in} - V_i}{R_1} \text{ and } I_F = \frac{V_i - V_0}{R_P}$$

Applying Kirchaoff's law at the inverting input we have $I1 = I_f + I^-$ where I^- is the current entering at the inverting input.

Now we assume that the OP-amp is ideal. The characteristics of an ideas OP-amp which are mecessary for out present purpose are :

(1) Input resistance, $R_i = \infty$, (2) Output resistance $R_0 = 0$, (3) Open loop voltage gain $A = \infty$, (4) Perfect balance, ie. V_0 = Owhum $V_1 = V_2$

As $R_i = \infty$, $I^- = 0$ $\therefore I_1 = I_f$

$$\frac{V_{in} - V_i}{R_i} = \frac{V_i - V_o}{R_f} \qquad \text{..... (1)}$$

Again for an ideal OP-amp amplifier A = ∞, That implies $V_i = -\frac{V_0}{A} = 0,$, Substituting this in eqn. (i) we get

$$\frac{V_{in}}{R_1} = \frac{-V_0}{R_f}$$

$$\frac{V_0}{R_{in}} = \frac{R_f}{R_1}$$

The ratio V_0/V_{in} is the voltage gain of the inverting amplifier circuit. It is called close loop gain of the amplifier. That means, it is the gain when operational ampklifier is used with feedback.

The gain is negative, as it should be for an investing amplifier. But more interesting thing is that magnitude of the voltage gain depends only on the ratio of the two resistances R_1 and R_f and not on the amplifier itself So, we can choose the two resistances to produce the required voltage gain.

Thermo emf is measured by operational amplifier. We need not know the inner mechanism of OP-amp. If is enough for our purpose to know that it is a voltage amplifying device. Which can produce an output voltage in the range of mV from the input of thermo emf, which is of the order of μV. The output voltage can be directly read by the voltmeter. One wire of the thermocouple is connected to inverting input terminal and the other wire is connected to the non-inverting terminal which is kept at zero potential by connecting to the ground. For example, for a copper constant thermocouple, the hot juncton is connected to the inverting terminal and the cold one to the non-inverting terminal.

It is voltage gain is A input voltage is V_{in}, Output is $V_{out} = AV_{in}$. Measuring V_{out}. We can know V_{in} (thermo emf).

13.3(ii) Theory

A thermo couple consists of two dissimialr metallic wires joined at their two ends to form a closed circuit. If one junction is at 0°C and the temperature (t°C) of the other junction is increased from zero. thermo emf (e), of teh order of micro-volt. Increases from zero according to the equation given by

$$e = at + bt^2 \text{ volt} \quad \text{..... (i)}$$

a & b are constants for a particular thermocouple thermo emf (e) at different temperatures (t) of the hot junction are measurd by an op-amp & e is plotted against t. The e–t curve so obtain is the calibration curve. As the temperature t is far away fro the neutral temperature, the calibration curve is part of the straight portion of parabolic (e–t) curve.

From the calibration curve we can find the thermoelectric power.

Thermoelectric power at temperature t is $p = \frac{de}{dt}$ = slope of the calibration curve at the poin corresponding to the temperature.

The temperature of the hot function at which e is maximum si called neutral temperature (t_o) when $t = t_n, \frac{de}{dt} = a + 2bt_n = 0, t_n = \frac{-a}{2b}$ ..... (ii)

To find neutral temperature, we require two experimental values of thermo emfs and corresponding temperatures : (e_1, t_1) and (e_2, t_2) we have

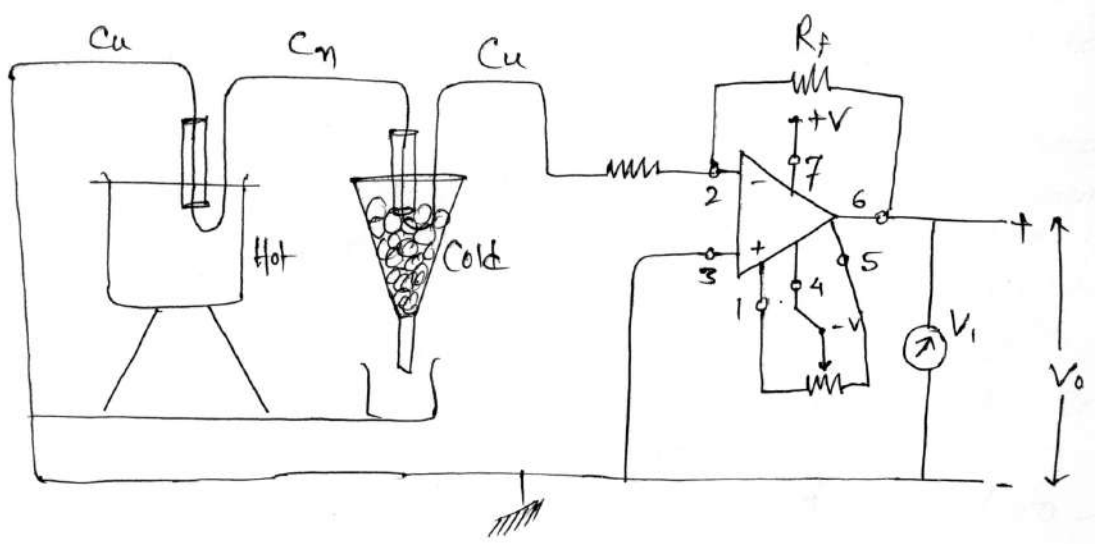
$e_1 = at_1 + bt_1^2$ & $e_2 = at_2 + bt_2^2$

from these two relation we get

$$a = \frac{e_1 t_2^2 - e_2 t_1^2}{t_1 t_2 (t_2 - t_1)} \& b = \frac{e_2 t_1 - e_1 t_2}{t_1 t_2 (t_2 - t_1)} \quad \text{..... (ii)}$$

We can find a and b uysing eqn. (iii) and neutral temperature for the couple can be calculated using eqn (ii).

To measure e by OP-amp, the required circuit is shown in Fig. For constant couple. Copper wire at the cold junction (–ve) is joined to inverting pin 2 through resistance R_1. The feedback resistance R_f is joined between pin 2 & pin 6. The hot junction of the couple is joined to the non-investing pin 3, which is eathed. The output voltage (V_0) is measured by the voltameter V_1. Pins 7 & 4 are Jaind to two power supplies +V –V respectively. To remove the off set voltage a potentiometer p is joined betwen pin 1 and 5 & its wiper is connected tot 4eh negative supply V.



13.4(ii) Apperatus

Thermocouple, power supply (+12V or +15V), IC OP AMP (IC 741), two resistance boxes, two keys ice bath containg melting ice & beaker containing water jobced over a tripod.

13.5(ii) Experiment Procedure

(1) Preparation of the thermocopule : Take two pieces of copper wire (Cu) and one piece of constants wire (Cn), each about one meter long. Clean the ends of the wires. Join one end of the constantan wire to one end of one copper wire and the other end of wire and the other end of the constantan wire to end of the other copper wires of twisting and then soldering the junctions with minimum of solder. Insert the copper wires into two thin glass tuber of lengths of about 25 cm, So that the two junctions rest at the lower ends of the glass tubes. Thus, we make it sure that copper and constantan wires do not touch each other at any points execpt at the two junctions.

(2) The circuit is completed as shown in Fig. Take resistance R_1 = 1 KΩ and R_f = 10 KΩ to get voltage gain 10. Exact values of the two resistances are determined by a multimeter.

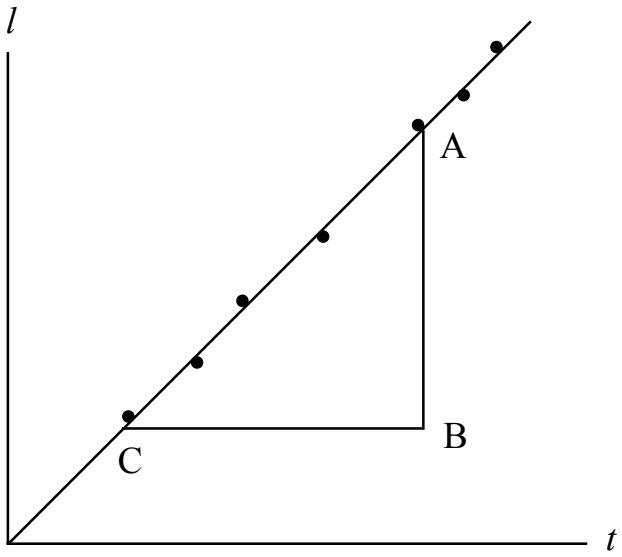
As the junction are now at the same (room) temperature, the output voltage, read by voltameter V_1 should be zero. If it is not zero, there is offset voltage./ To remove the offset voltage the wiper of the potentiometer P is rotated in the right direction to make the output voltage zero.

(3) Now the junction, which is comected to the inverting pin, is placed in the ice bath, containing metting ice. The other junction, whihc is connected to the non inverted pin is placed in the water kept in a beaker placed over a tripod. From a stand a thermometer T, reading $^1/_{10}$th of a degree, is placed inside the water, with its bulb close to the junction. With the help of separtate clamps, the two junctions are kept field in their positions, equally surrounded by melting ice and water respectively.

(4) After waiting for some time, note the temperature (t) of the water in the beaker, which should steady for at least 2 min. Note the output voltage (V_0) read by the voltameter V_1. Now start hearing the Water and raise the temperature by 8 to 10°C. Hold the temperature steady for 2 mins and note the temperatrue (t) and the corresponding output voltage (V_0). Continue such observations by increasing the temperatrues by steps of 8 – 10°C until it rises upto about 95°C, Calculate the input voltage (V_{in}) in lach case.

Which is the therm emf (e). $\therefore V_{in} = e = \frac{R_i}{R_f} V_0$.

(5) Plot e along y-axis and t along x-axis in a graph paper. Keeping the origin at (0, 0) as origin is a sure point of the curve. choose the scales along the two axes such that the whole of the given graph paper is utilised. Draw the mean the through the origin about which the experimental points are enenly distributed. This is the calibration curve. Thermodectric power P = slop of ther curve AB/BC.



(6) To calculate neutral temperatrue choose any pair of the measured values (e_1, t_1) (e_2, t_2) and Find the values a & b of the thermocouple by eqn. (iii) From these values find the nutral temperature t_n from eqn (ii) Repeat ther same calculation, if time permits, for other pairs, calculated the mean value.

13.6(ii) Experiment Results

A. Resistance put in the resistance boxes R_1 & R_f :

R_1 = 1 KΩ & R_p = 10 KΩ

Measured values : R_1 = ... KΩ & R_p = ... KΩ

∴ Voltage gain = $\frac{R_f}{R_1}$ = ...

B. Off set voltage is removed by rotating the wiper of the potentiometer.

C. Data for (e – t) graph & duauring of the calibration curve

Table 1

Temperature of the cold junction = 0°C

No of obs	Temp. of the hot junction t°C	Amplified output voltage V_0 mV	Thermo emf $l = \frac{R_1}{R_f} V_0$ mV
1 2 3			

D. Deter,omation of thermoelectric power (P)

From Fig. $P = \frac{AB}{BC}$ = — = ...V/°C

E. Determination fo nutral point :

For a pair of measured emf δ

(e_1 = mV, t_1 = ... °C), (e_2 = ... mV, t_2 = ... °C

$$a = \frac{e_1 t_2^2 - e_2 t_1^2}{t_1 t_2 (t_2 - t_1)} \text{ mV/°C and } b = \frac{e_1 t_1 - e_2 t_2}{t_1 t_2 (t_2 - t_1)} \text{ mV/°C}$$

Neutral temp $t_n = -\frac{a}{2b} = \frac{.....}{2x.....} = ...°C$

No of Obs	Temp of the hot junction t°C	Thermo emf e from Table-1 mV	Neutral temp t_n°C	Mean t_n°C
1		.....	[for obs 1 & 2]	
2		.....		
3		.....	[for obs 2 & 3]	

13.7(ii) Discussion

1) Identification of the different pin numbers of op-amp is very important. Take help of the teacher and suritch on the circuit only after it is inspected by teachers.
2) Resistaces R_1 and R_2 should be measured very accurately by a multimeter.
3) Cold junction should be cheaked from time to time by pressing the powered ice with a glass rod and adding more ice as and when nesersary.
4) Tempratrue of hot water should be kept steady for at least 2 mins, before reading of voltameter is taken.
5) Temperatrue of the hot function should not exceed the boiling point of water to get a straight calibration curve.

13.8(ii) Summary

From the induystrial view point, temperature measurement is one of the important measurements. The resistance temperature detector (RTD) and thermocouple (T_c) are the major device of the temperature measuring instrument. Temperature measurment is important for monitoring and control purposes.

13.9(ii) Exercise and Answer

1. What will happen when two wires of two different metals are joined at their ends and a difference of temperature is maintained between the two function?

Ans. A current will flow in the circuit. which is known as the thermo-current and this phenomenous is called seebeck effect.

2. What will happen if a cell is inserted in the thermo-couple circuit whose two junctions are kept at the same temperature?

Ans. One of the junctions will be hot while the other junction will be cold. This phenomenon is known as peitier effect.

3. What will happen when a temperatrue difference is maintained between the two points of one conductor of a thermo couple?

Ans. A potential difference will be set up between the two points of the same conductor having a difference of temperature. This phenomenon is known as Thomson effect.

4. What is the difference betwen peltier effect and Joule effect?

Ans. Heating in peltier effect is proportional to the current while heating in Joule effect if proportional to the square of the current.

5. What is neuitral temperature of a couple?

Ans. If is the temperature of the hot function of which the thormo emf generated in the couple is maximum.

6. What is the relationship between the thermo emf (e) and tem (t) of the hot junction when that of cold junction is 0°C?

Ans. Within a small range of temperature the relation between e and t can be represented by $e = at + bt^2$ or $a = at^6$.

7. What do you mean by thermo-electric power?

Ans. Thermo electgric power of a couple at a particular temperature is the increase of the thermo emf when the temperature of the hot junction is increased by 1°C. If dF be the increase of thermo emf for a rise of temp. dT° at a temp. T of ther hot junction then thermo electric power at T° is $\frac{dE}{dT}$.

8. What is the nature of the curve connecting thermo electric power P = $(\frac{dE}{dT})$ & temperature?

Ans. It is a straight line. The slope of this curve may be +Ve or –Ve.

9. What is pyro-electricity?

Ans. It is an electrical effect in which certain crystals, especially tourmaline electrical sharges when heated or coded.

10. What is an inversion temperature?

Ans. It is the temperature of the hot junction at which thermo emf is zero & is about to be reversed.

11. Can you measure the thermo emf by using a microvoltmeter?

Ans. No, by using avoltmeter we get p.d and not emf.

12. What type of galvanometer is suitable for this experiment?

Ans. A suspended coil dead beat and voltage sensitive type.

13. Why do you use a potentiometer and not a voltameter to measure the thermo emf?

Ans. In potentiometer we take reading at null condition, when no current flows through the thermo couple. Hence the measurement become accurate. A voltmeter measures p.d. and not the emf.

14. What is the value of thermo electric power at neutral temperature?

Ans. Zero.

Unit 14 ❑ To design Fourier spectrum of (i) square (ii) triangular and (iii) half sinusoidal wave form by CRO

Structure

14.1 Objective

To understand Fourier series representation of periodic signals.

14.2 Introduction

Fourier's theorem states that a periodic function can be expressed by an infinite series of sine or cosine functions of hermonically related frequencies. The frequency of the sine or the cosine term in the infinite series is a harmonic of the frequency of the periodic function.

14.3 Theory

Figure (i), (ii), (iii) and (iv) respectively show form periodic waves namely (i) a square wave of period T and amplitude V_1 (ii) a triangular wave of period T and peau

value V_1 (iii) a half finersoidal wave (which is the output of a half wave rectifier driven from a sincesoidal source) of period T and amplitue V and (iv) a half sinusoidal (which is the output of a half wave rectifies driven from a sinusoidal source) of period T and amplitade V.

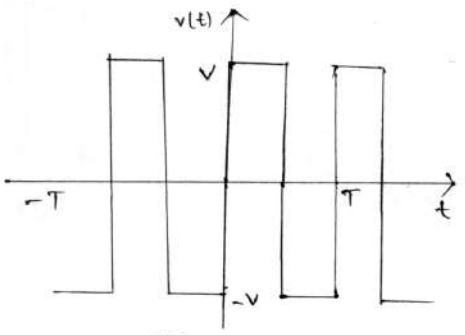


Fig. 14 (i)

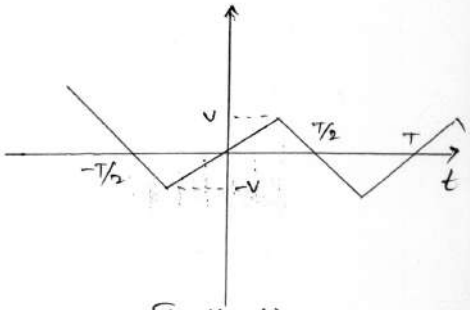


Fig. 14 (ii)

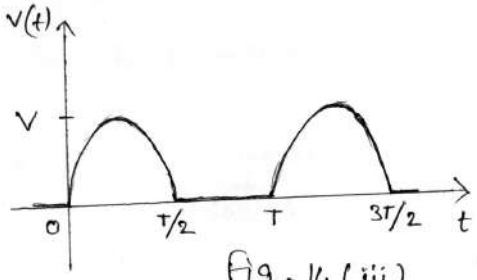


Fig. 14 (iii)

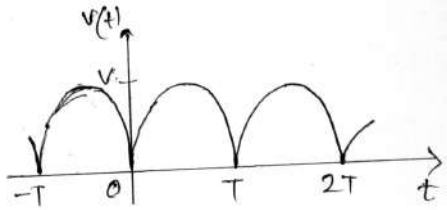


fig. 14 (iv)

$$A_0 : A_1 : A_2 : A_4 = 1 : \frac{\pi}{2} : \frac{2}{3} : \frac{2}{15}$$

The corresponding amplitude spectrum is shown in fig. 14 (vii). Considerily the AC components.

$$A_1 : A_2 : A_4 = 1 : \frac{4}{3\pi} : \frac{4}{15\pi}$$

For the half sinusoidal waveform of Fig. 14 (iv), the dc compact is $A_0 = \frac{2V}{\pi}$, the amplitude are $2f_0$, $4f_0$, $6f_0$.

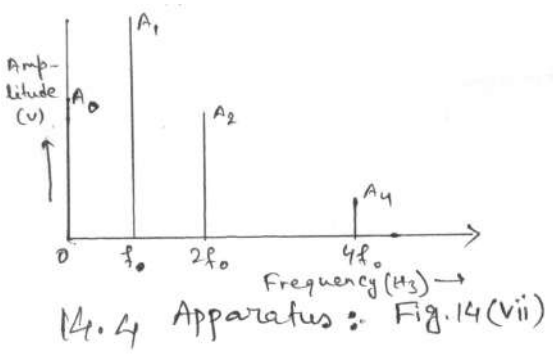
$$A_2 = \frac{4V}{3\pi}, A_4 = \frac{4V}{15\pi}, A_6 = \frac{4V}{35\pi}$$

$$A_0 : A_2 : A_4 : A_6 = 1 : \frac{2}{3} : \frac{2}{15} : \frac{2}{35}$$

The amplitude spectrum of the half simutiodal waveform is shown in Fig. hence considering the ac component only

$$A_2 : A_4 : A_6 = 1 : \frac{1}{5} : \frac{3}{35}$$

As the amplitude doop off repidly with increasing frequency, the first few frequency components are significant.



14.4 Apparatus : Fig. 14 (vii)

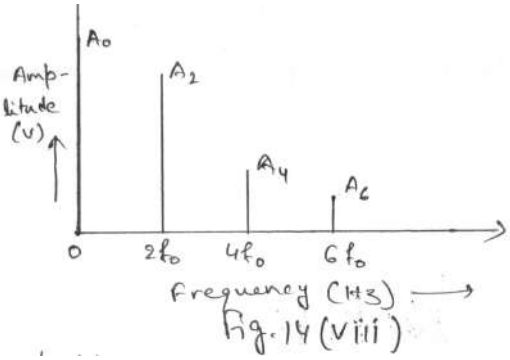


Fig. 14 (viii)

14.4 Apparatus

(i) Function Generator giving square and triangular waveforms.

(ii) Half wave and full wave rectifiers giving half sinersoidals.

(iii) Several active based pass filters (A detailed fiscussion of these filters and their design can be found in the book "Fundamental of Electric cicuit Theory by D. Chattopadhyay and P.C. Rakshit (S chand and Co New Delhi).

(iv) A CRO

(v) Connecting wires etc.

14.5 Experimental Procedure

1. Obtain a square wave form the function generator and display it on a CRO. Choose a suitable frequency, say 1 kH2 of the wave form.

The Fourier series expansions of the four periodic waves are given by

(i) $V(t) = \frac{4V}{\pi} \sum_{n=1,2,3,5...}^{\infty} \frac{1}{n} \sin n\omega_0 t$

(ii) $V(t) = \frac{8V}{\pi^2}\left[\sin \omega_0 t - \frac{1}{9}\sin 3\omega_0 t + \frac{1}{25}\sin 5\omega_0 t \ldots..\right]$

(iii) $V(t) = \frac{V}{\pi} + V\left(\frac{1}{2}\sin \omega_0 t - \frac{2}{3\pi}\cos 2\omega_0 t - \frac{2}{5\pi}\cos 4\omega_0 t \ldots..\right)$

(iv) $V(t) = \frac{2V}{\pi} + \frac{4V}{\pi} \sum_{n=2,4,6...}^{\infty} \frac{\cos n\omega_0 t}{1-n^2}$, where $\omega_0 = \frac{2\pi}{T}$ is the fundamental angular frequency v.

The plot of teh amplitude of the harmonic components of teh Fourier series with frequency is known as teh amplitude spectrum of the waveform. For the square wave of Fig. 4 (i), the amplitudes of the frequency components $f_0 = \omega_o/2\pi$. $3f_0$ and $5f_0$ are respectively.

$$A_1 = \frac{4V}{\pi}, A_3 = \frac{4V}{3\pi} \text{ and } A_5 = \frac{4V}{5\pi} \text{ so that } A_1 : A_3 : A_5 = 1 : \frac{1}{3} : \frac{1}{5}$$

The amplitude spectrum of teh square wave is depicted in Fig. 3.EL32(V)

For the triangular wave the amplitudes of the frequency components f_0, $3f_0$ and $5f_0$ respectively.

$$A_1 = \frac{8V}{\pi^2}, A_3 = \frac{8V}{9\pi^2}, A_5 = \frac{8V}{25\pi^2}$$

$$A_1 : A_3 : A_5 = 1 : \frac{1}{9} : \frac{1}{25}$$

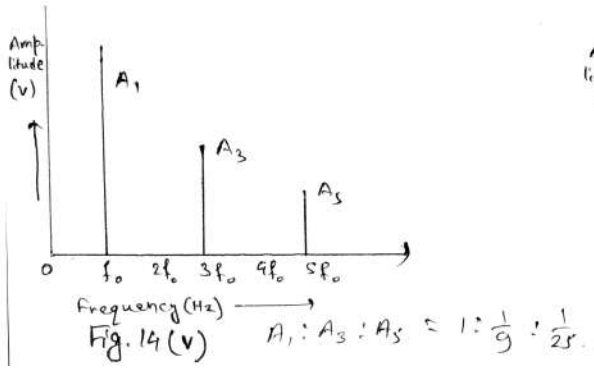


Fig. 14 (v) $A_1 : A_3 : A_5 = 1 : \frac{1}{9} : \frac{1}{25}$

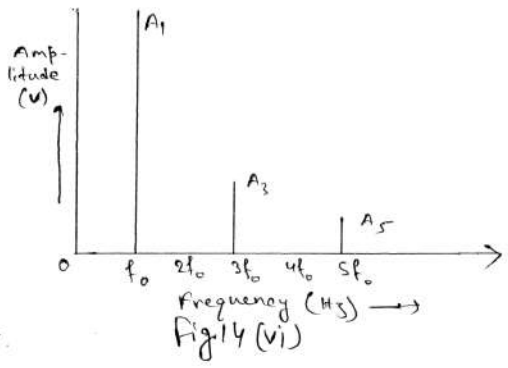
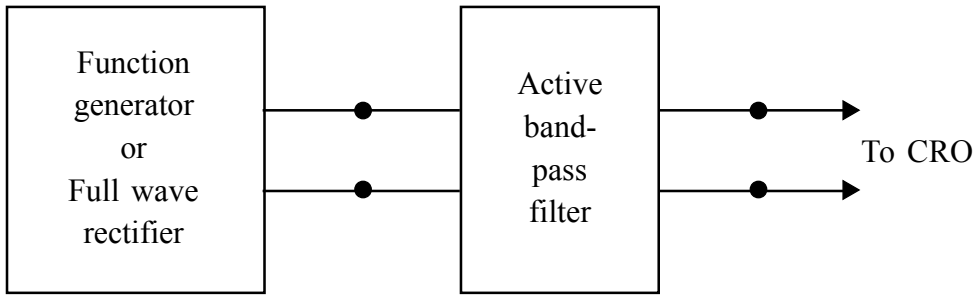


Fig. 14 (vi)

The amplitude spectrum of the triangular wave is displayed.

For the half sinusoidal of Fig. the dc compenent is $A_0 = \frac{V}{\pi}$. The amplitude of the frequency components f_0, $2f_0$, $4f_0$ are $A_1 = \frac{V}{2}, A_2 = \frac{2V}{3\pi}, A_4 = \frac{2V}{15\pi}$.

2. Take a band-pass filter of centre frequency 1 KHz and of narrow bandwith and set up the circuit as in Fig. 3.EL32(ix). The band-pass filter allows only the frequency component f_0(= 1.KHz) to pass through and rejects all other frequency from appearing at its output.



3. Display the output singal of the band-pass filter on the CRO and measure its amplitude A_1 by the CRO.

4. Replace the band-pass filter successfully by band. pass filters of centre frequencies $2f_0$, $3f_0$, $4f_0$ and $5f_0$ and measure by CRO the corresponding amplitudes A_2, A_3, A_4 and A_5. Correct the amplitudes by the gains of the active band-pass filters at the centre frequencies.

5. Plot the amplitude spectrum as in Fig. 3.EL32(V) and find $A_1 : A_3 : A_5$. Compare it with the tgheoretical value.

6. Repeat the experiment for a triangular wave form of frequency f_0 = 1 KHz, say.

7. Replace the function generator by a half-wave rectifier giving a half sinusoidal wave form of frequency f_0 = 1 KHz. and repeat the experiment. The dc component of Fourier expansion of half sinusoidal waveform is not considered here only A_1, A_3 and A_4 are measured by the CRO.

8. Repeat the experiment by replacing the half wave rectifier with a full-wave rectifier. Measure A_2, A_4 and A_6.

14.6 Experimental results

Table 1

Results for a square wave

f_0 = ... Hz.

Frequency components (Hz)	Amplitude (volt)	$A_1 : A_3 : A_5$		Remarkes
		Experimental	Theoritical	
... (= f_0)	... (= A_1)			
... (= $2f_0$)	... (= A_2)			
etc	etc			

Make simular tables for triangular and half sinusoidal wave forms.

14.7 Discussions

1. The CRO must be operated in the triggered mode so the pattern on the screen is steady.
2. If the gains of the active band-pass filters at the centre frequencess are equal, the amplitudes need not be corrected for these gains, since the gains cancel out the taking the amplitude ratios.

14.8 Summary

In this method, the frequency of the input wave form is changed keeping the resonant frequency of the tuned circuit constant. The frequency must be varied slowly and carefully to get a maximum amaplitue of the output sine wave across the tuned circuit. The input waveform should be free from appreciable distortion. Otherwise, the agreement between the theory and the experiment will not be satisfactory

14.9 Exercise and Answer

1. State Fourier's theorem.

Ans. See 'Theory'.

2. What are Dirichlet's conditions?

Ans. The sufficient conditions required for the periodic function f(t) to express it as a convergent Fourier series are called Divichlet's conditions.

The conditions are : (i) f(t) is single valued and finite, (ii) f(t) has a finite number of finite discontinuities in the period T_s, (iii) f(t) has a finite number of maxima and minima in the interval T_1 and $\int_{t_0}^{t_0+T} |f(t)|\,dt$ exists.

3. What are the amplitude and phase spectra?

Ans. The Fourier seried of a periodic function can be expressed in the following form.

$$f(t) = A_o + \sum_{n=1}^{\infty} A_n \cos(nw_o t - O_n)$$

where A_o is constant, and A_n and O_n are respectively the amplitude and the phase of the nth hermonic. The variation of A_n with n(or nw_o) is called the amplitude spectrum, and the variation of O_n with n(or nw_o) is known as the phase spectrum of teh signal f(t).

4. What do you mean by even-function symmetry, odd-function symmetry, and have wave symmetry?

Ans. The periodic function f(t) is said to process even-function symmetry if f(t) = f(–t). The function f(t) has odd-function symmetry if f(t) = –f(–t). The periodic function is said to have helf-wave symmetry if $f(t) = -f(t - {}^{T}/_{2})$.

5. What is the effective (or nms) value of the periodic function f(t)?

Ans. It is given by

$$F_{eff} = \sqrt{\frac{1}{T}\int_0^T \left\{f(t)^2\right\}}dt$$

6. What is parallel resonance?

Ans. Resonance accuring in a circuit containing an inductor in parallel with a capacitor, is called parallel resonance and the circuit is referred to as a parallel resonant circuit. parallel resonance is also called anti-resonance.

7. What is the quality factor Q of a parallel resonant circuit?

Ans. Since the capacitor losses are very small, their Q-values are very high. So the Q of a parallel resonant circuit is given by Q of the inductor coil at resonance, i.e. $Q = \frac{w_o L}{R}$, where R is the resistance of the coil.

8. What is the capacitor current at resonance?

Ans. It is Q times the current delivered by the generator. Thus the circuit gives current magnification.

9. What is the resistance and the reactance offered by the parallel resonant circuit at resonance?

Ans. The resistance is the dinamic resistance r_d and the reactance is zero.

10. When do you say that a circuit is resonent?

Ans. The circuit is resonant when the current and the voltage are in phase, i.e., the power factor is unity.

11. Why is the parallel resonent circuit called a rejector circuit?

Ans. As the inductor resistance $R \to 0$, the dinamic resistance $r_d \to \infty$. So, the source current is a minimum at the parallel resonant frequency f_p. The source current increases as the frequency changes from f_p on either side. So, if the source contains a large number of frequency components, the circuit rejects the frequency equal to its resonant frequency f_p by drawing minimum current from the source from the source. Hence the parallel resonant circuit is called a rejector circuit.

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